FIG. 1

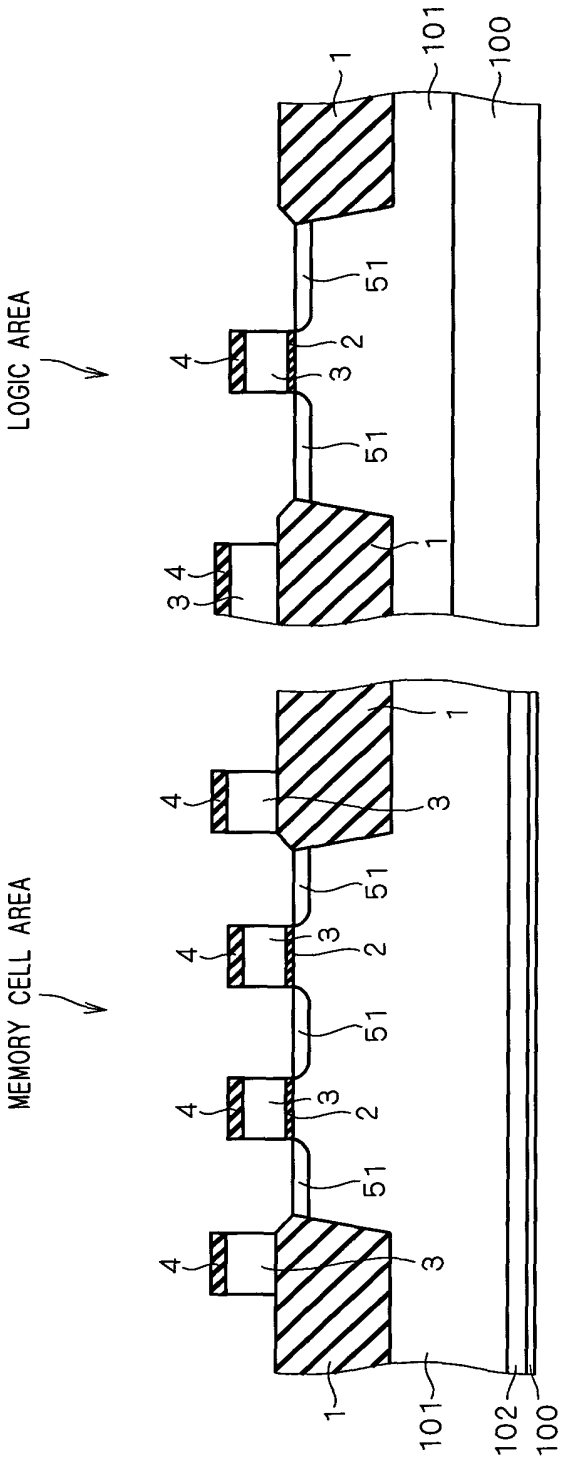


FIG. 2

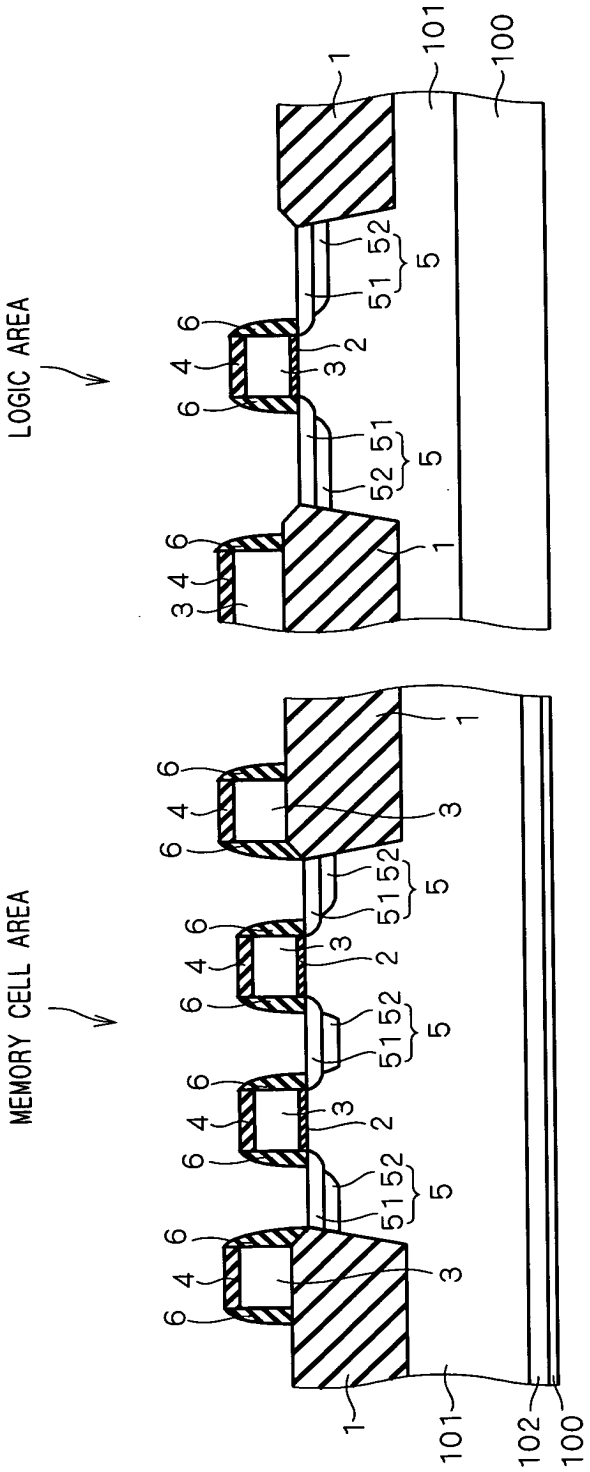


FIG. 3

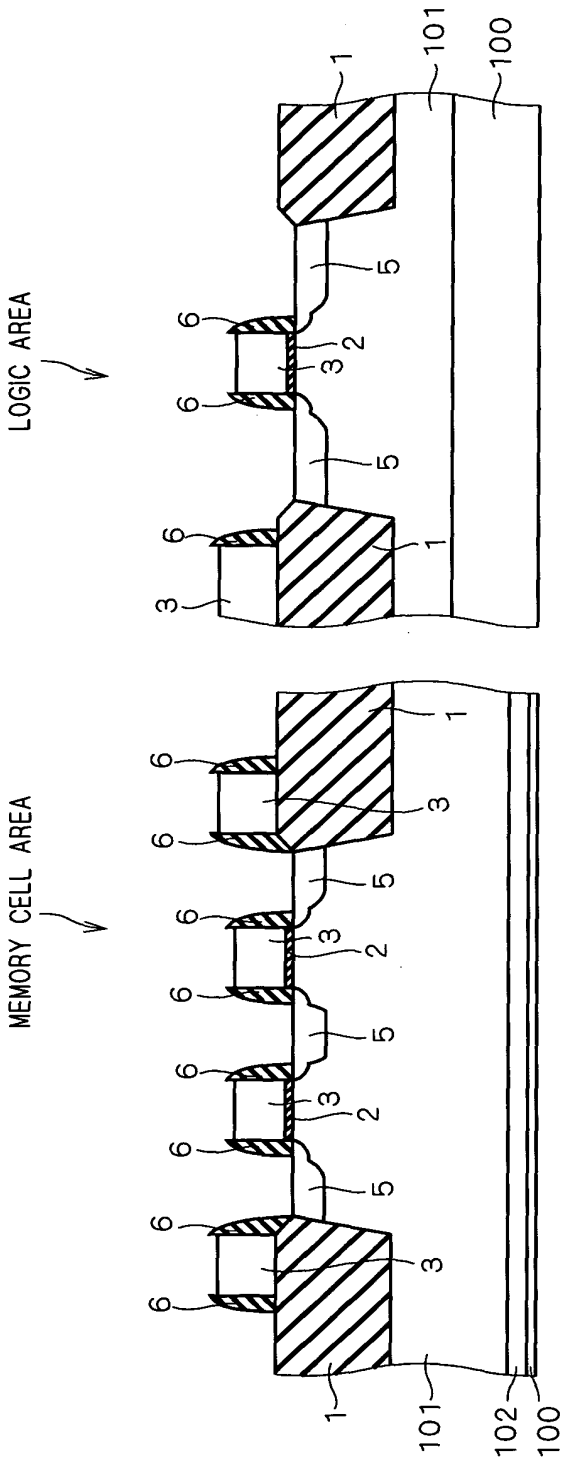


FIG. 4

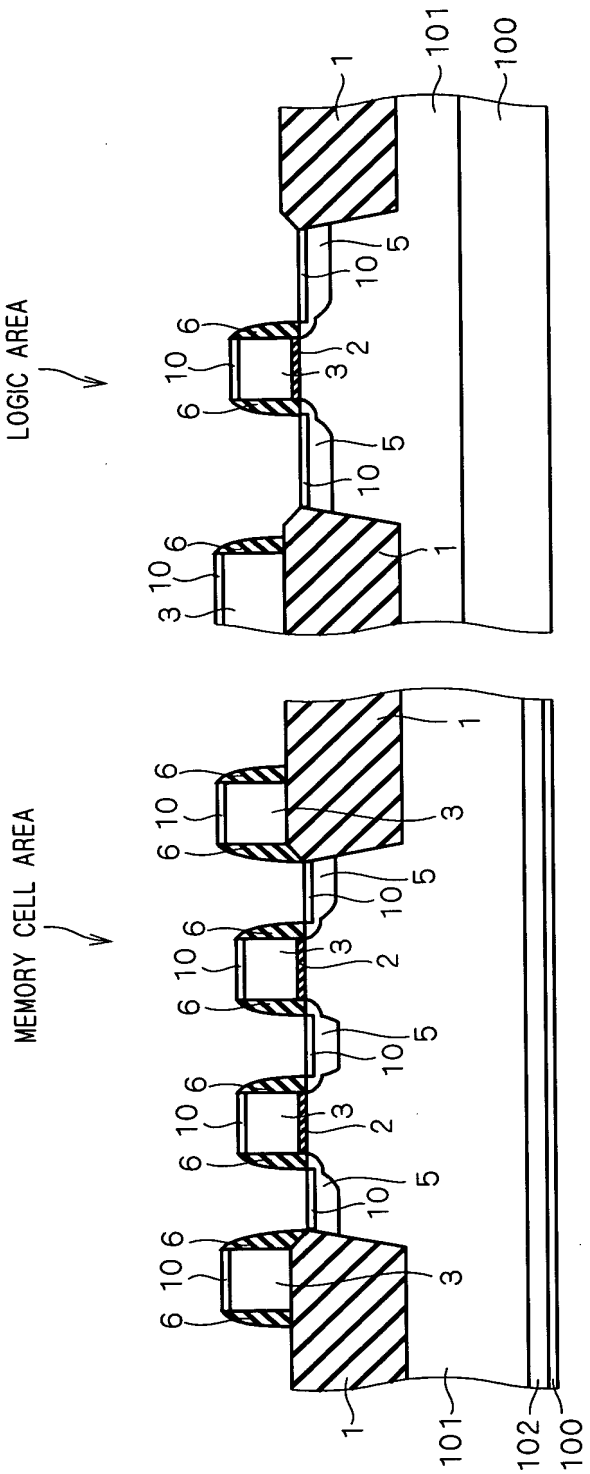


FIG. 5

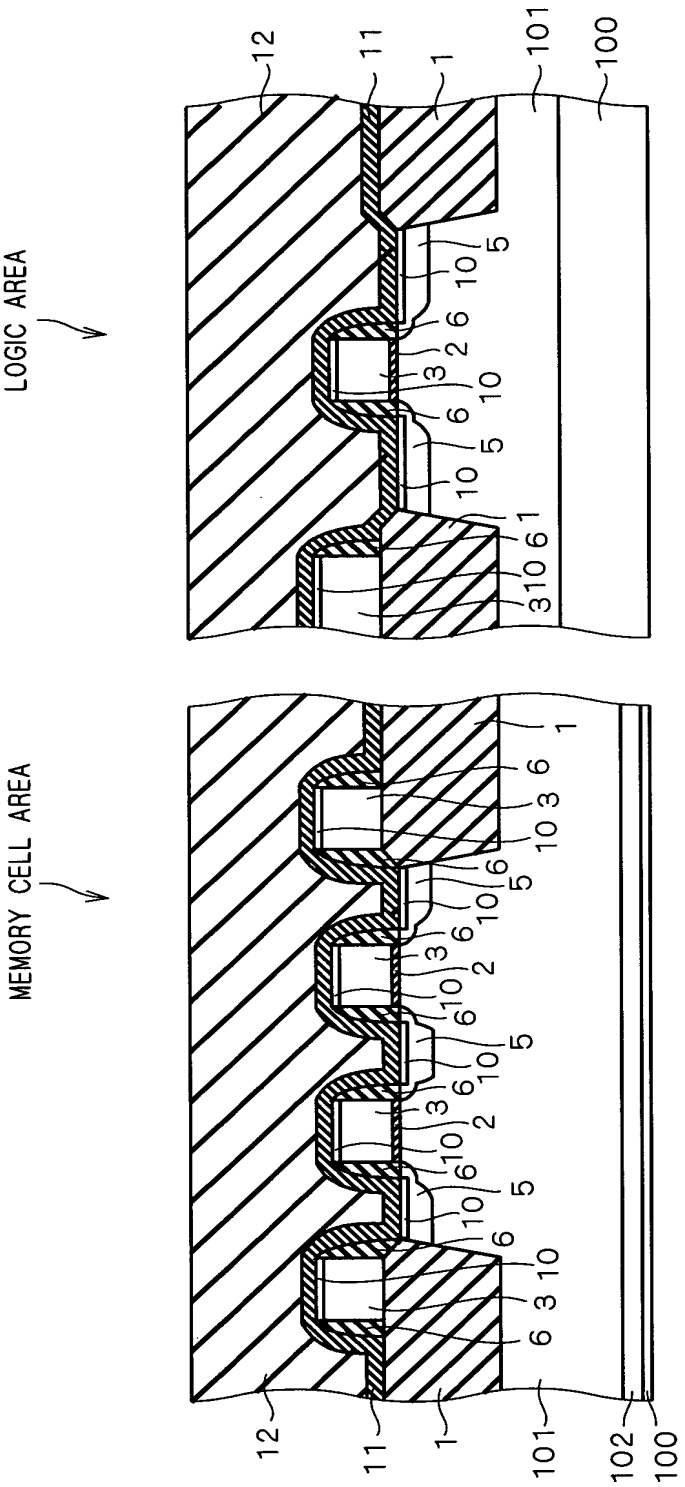


FIG. 6

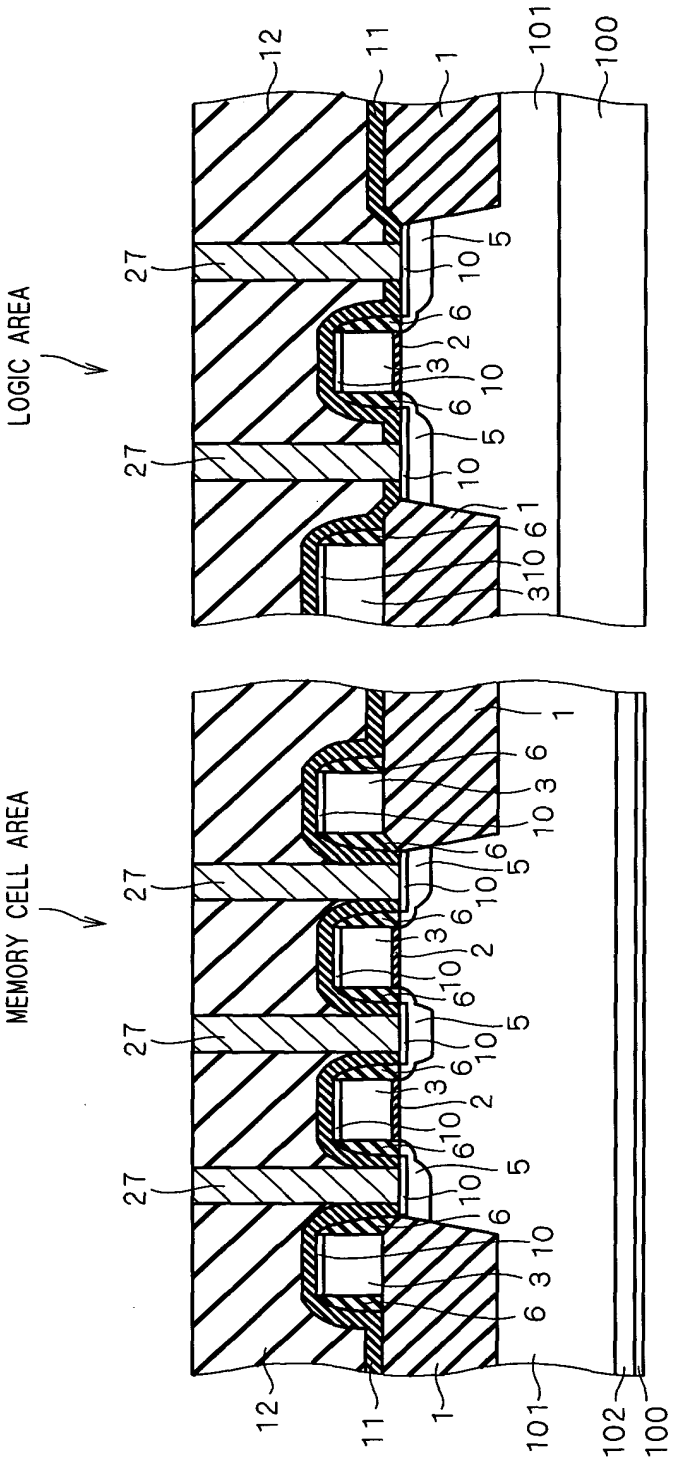


FIG. 7

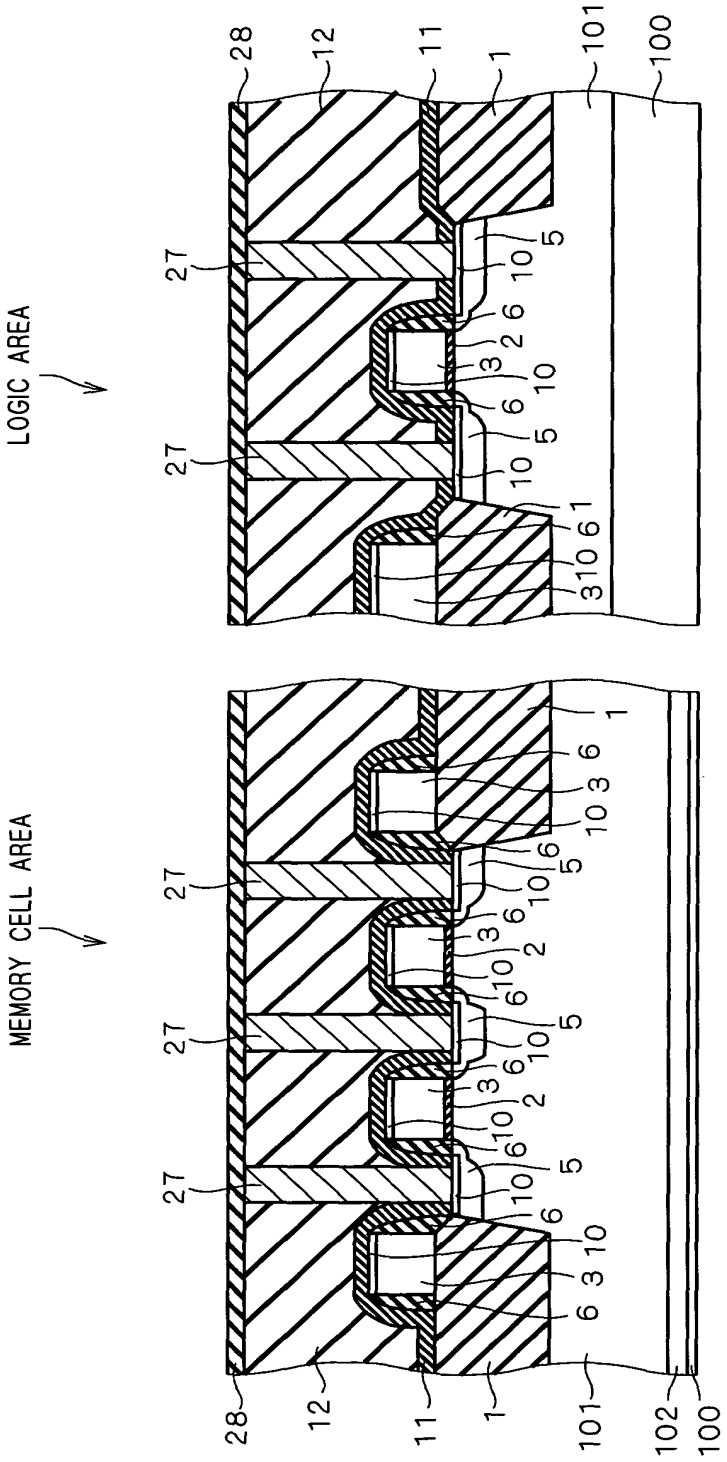

LOGIC AREA
MEMORY CELL AREA
28
12
11
1
101
100
27
5
10
6
2
3
10
6
5
10
6
1
3
10
6
10
3
6
5
10
6
3
2
10
6
10
5
6
3
2
10
6
10
5
6
10
3
6
10
3
6
28
12
11
1
101
102
100

FIG. 8

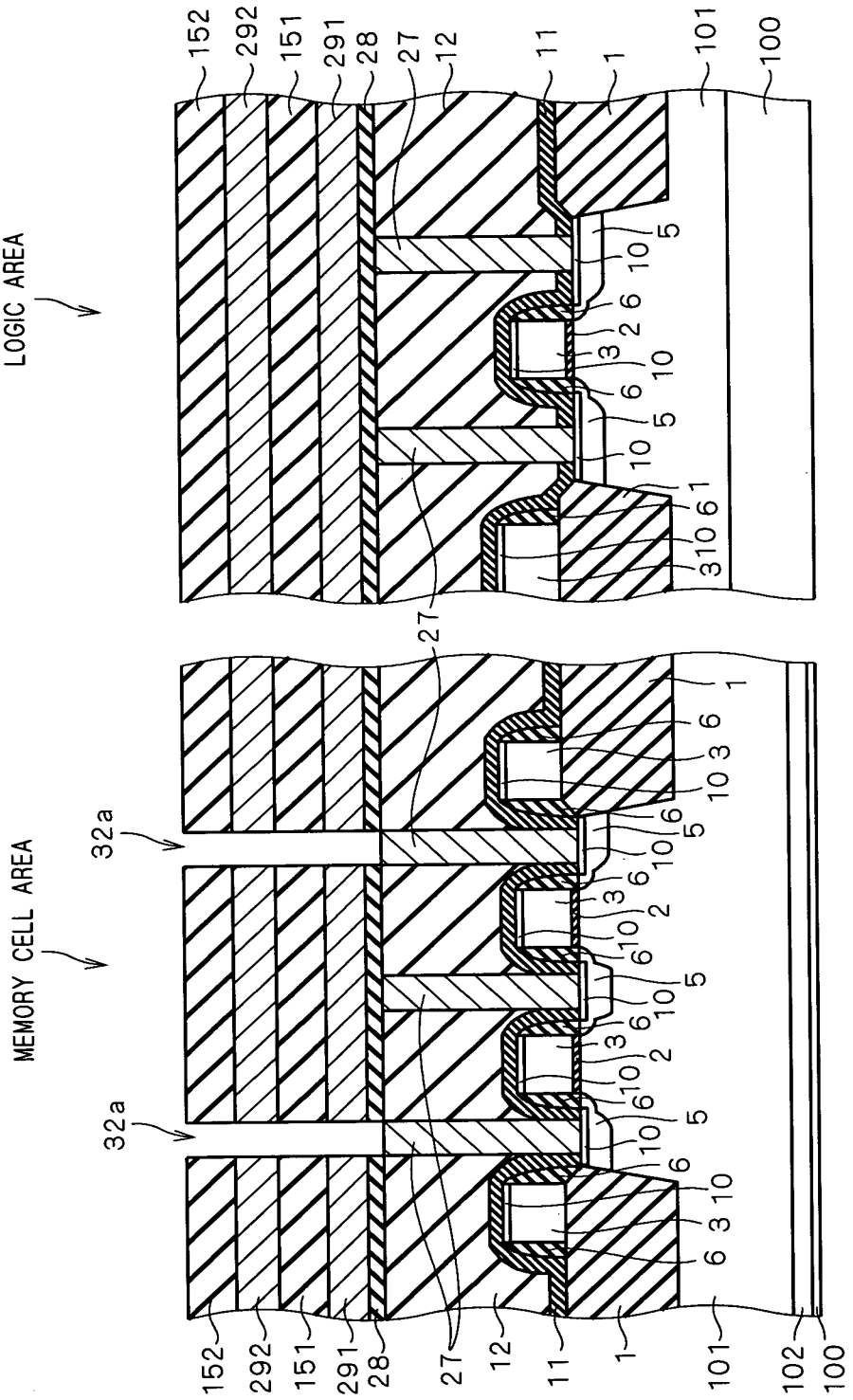

LOGIC AREA
MEMORY CELL AREA
32a
32a
152
292
151
291
28
27
12
11
1
101
102
100

FIG. 9

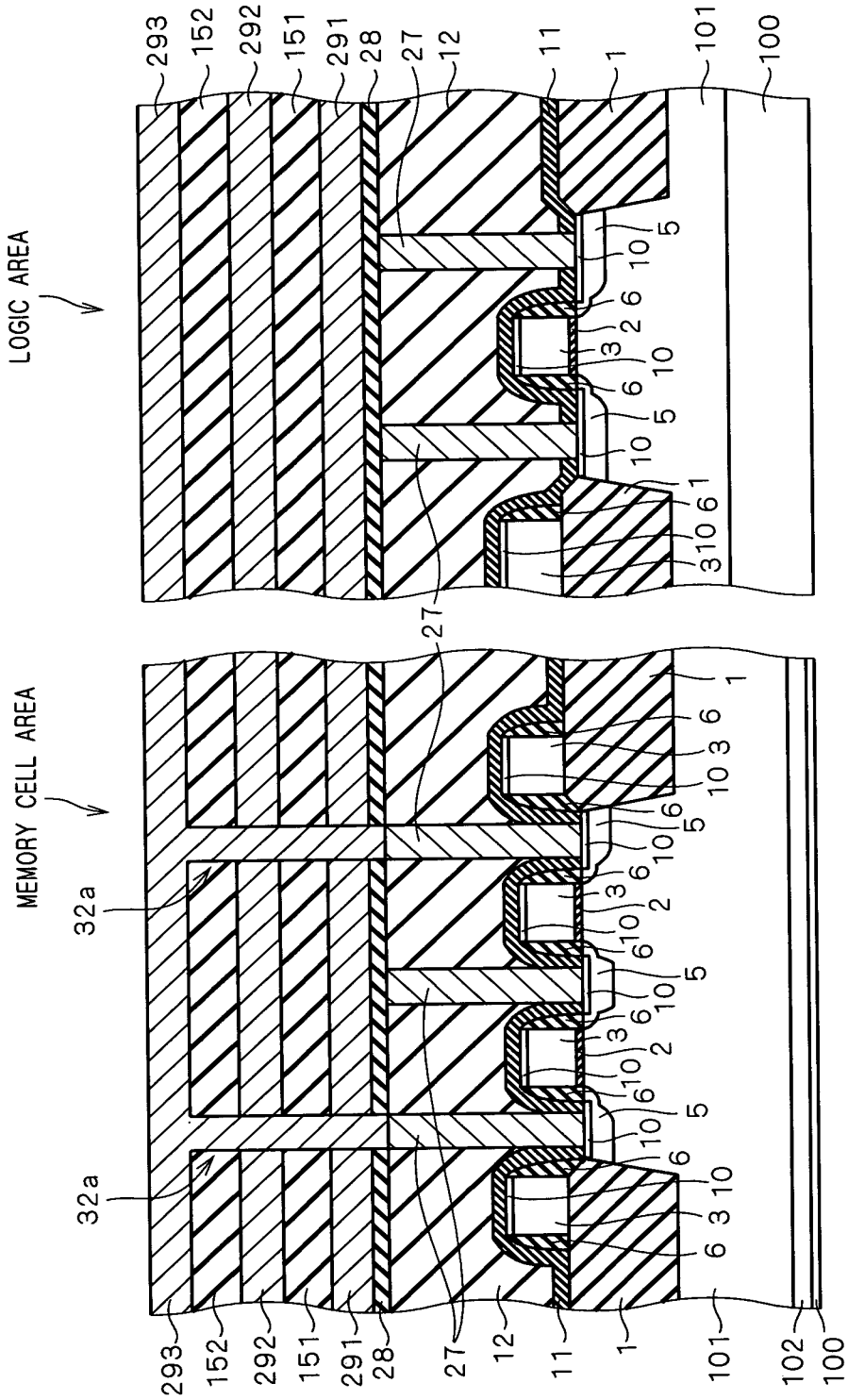

LOGIC AREA
MEMORY CELL AREA
32a
32a
293
152
292
151
291
28
27
12
11
1
101
102
100

FIG. 10

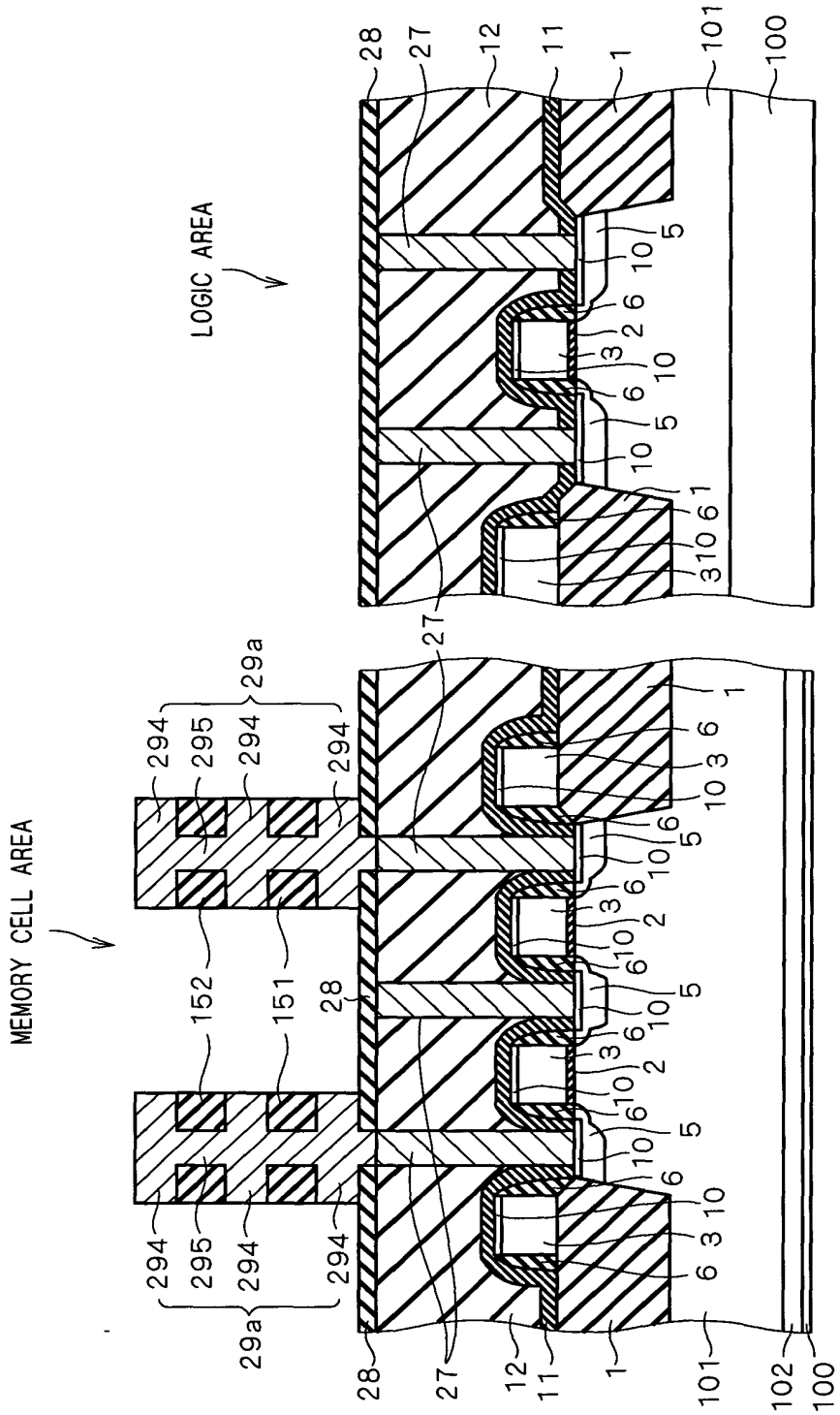

MEMORY CELL AREA
LOGIC AREA
28
27
12
11
1
101
100
102
29a
294
295
152
151
10
6
5
3
2

FIG. 11

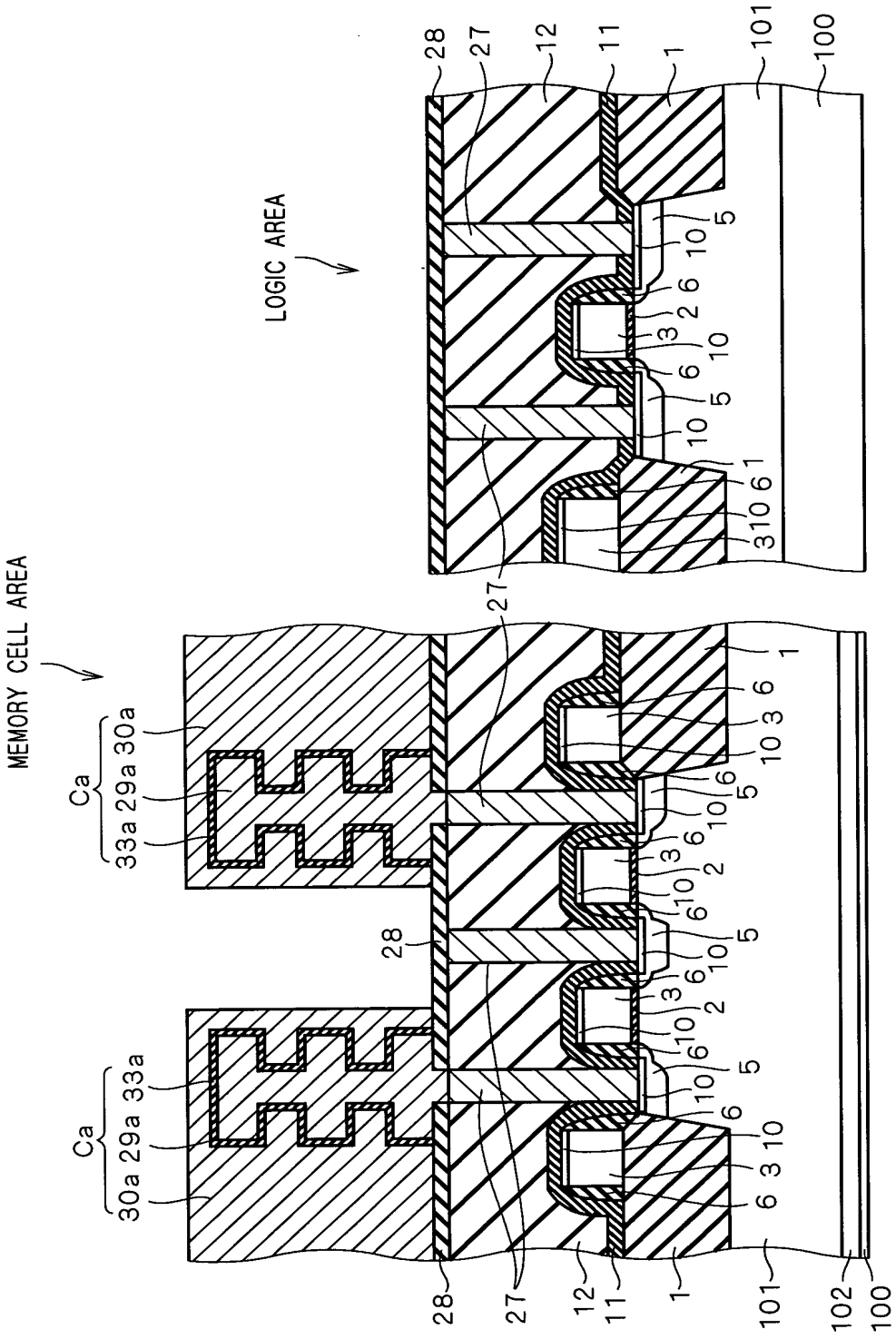

MEMORY CELL AREA
LOGIC AREA
Ca
30a 29a 33a
33a 29a 30a
28
27
12
11
1
101
102
100
2
3
5
6
10

FIG. 12

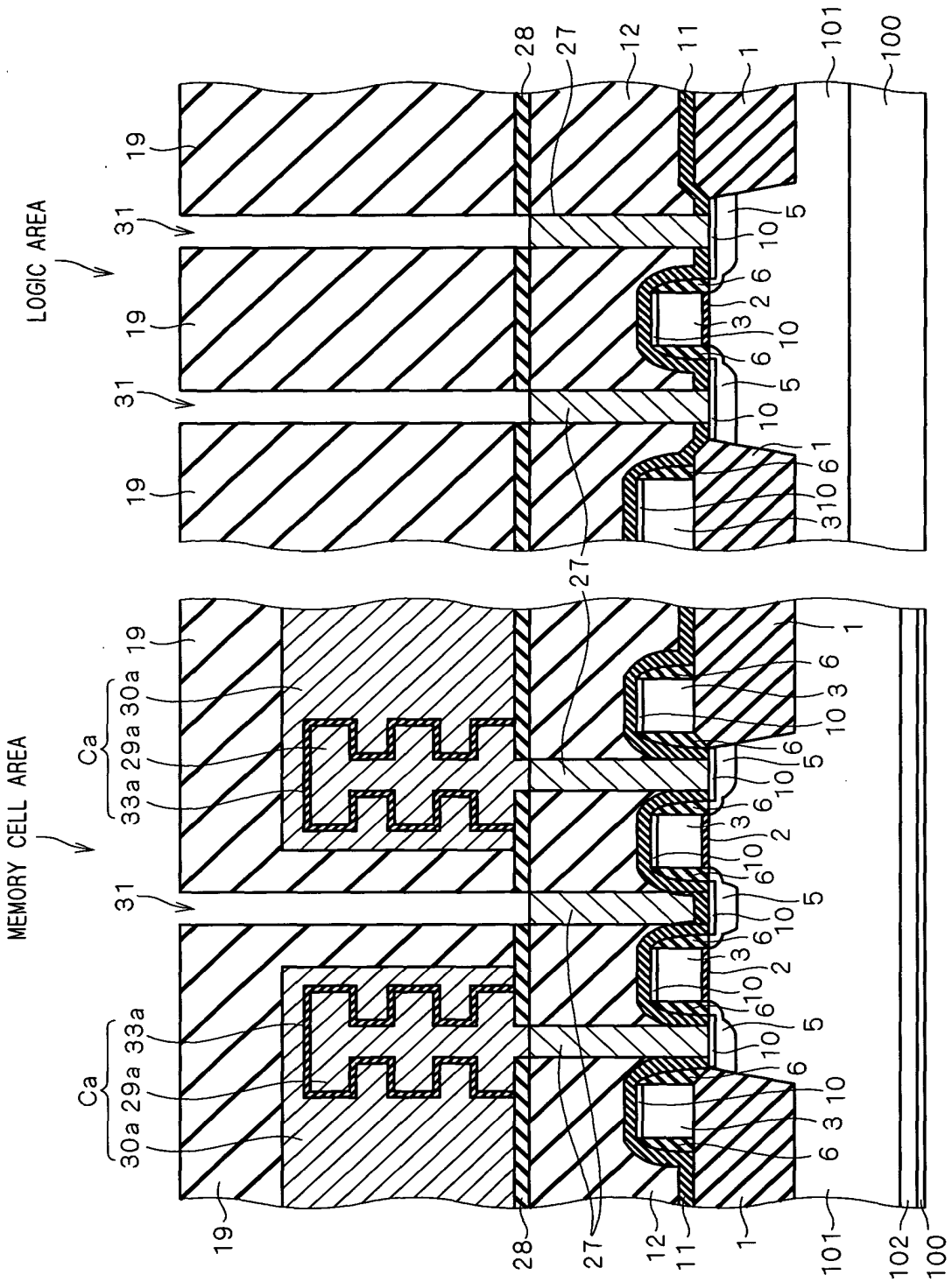

LOGIC AREA
MEMORY CELL AREA
Ca
19
31
30a
29a
33a
28
27
12
11
1
101
102
100
2
3
5
6
10

FIG. 13

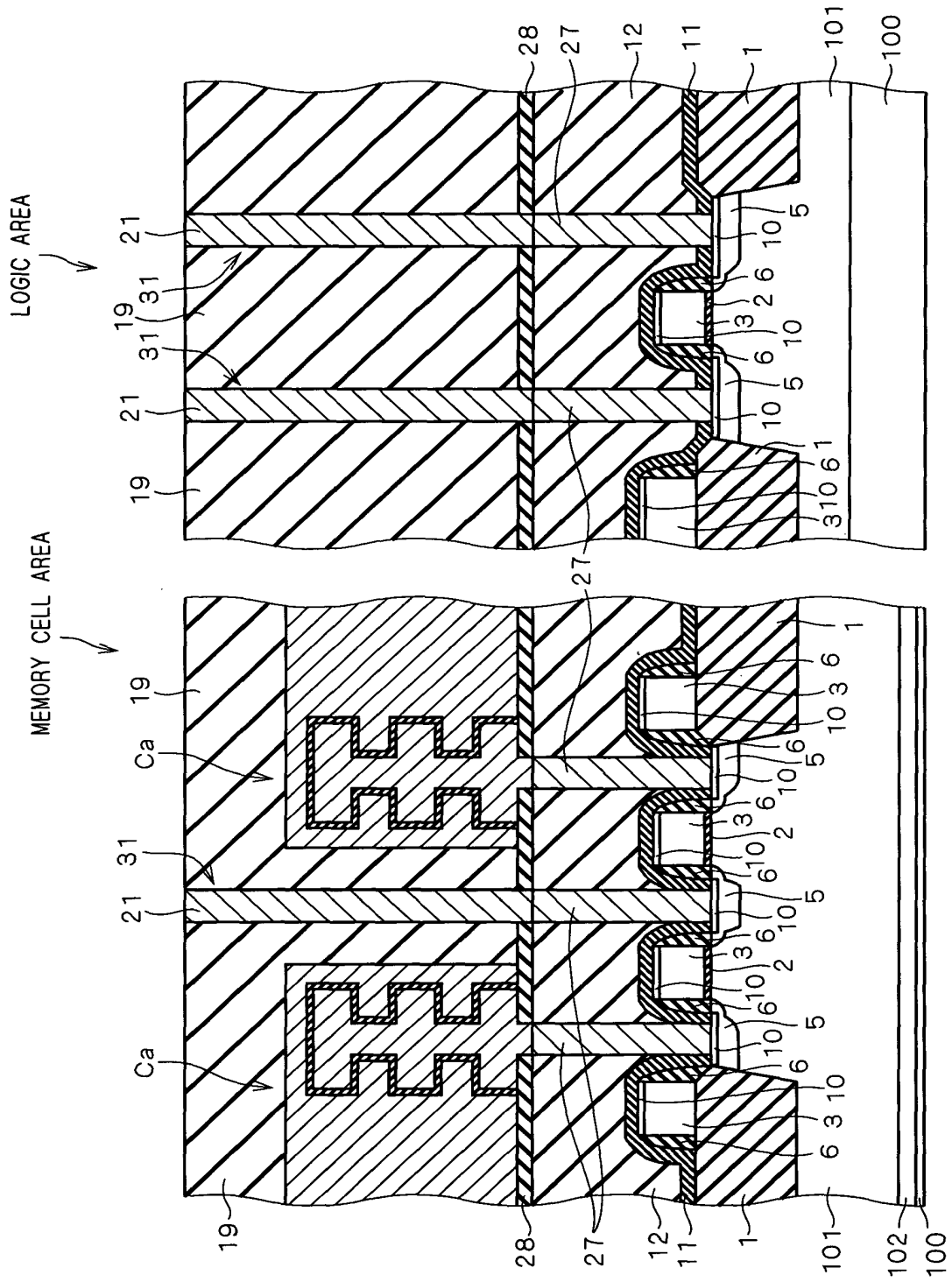

LOGIC AREA
MEMORY CELL AREA
Ca
Ca
19
21
31
28
27
12
11
1
101
100
102

FIG. 14

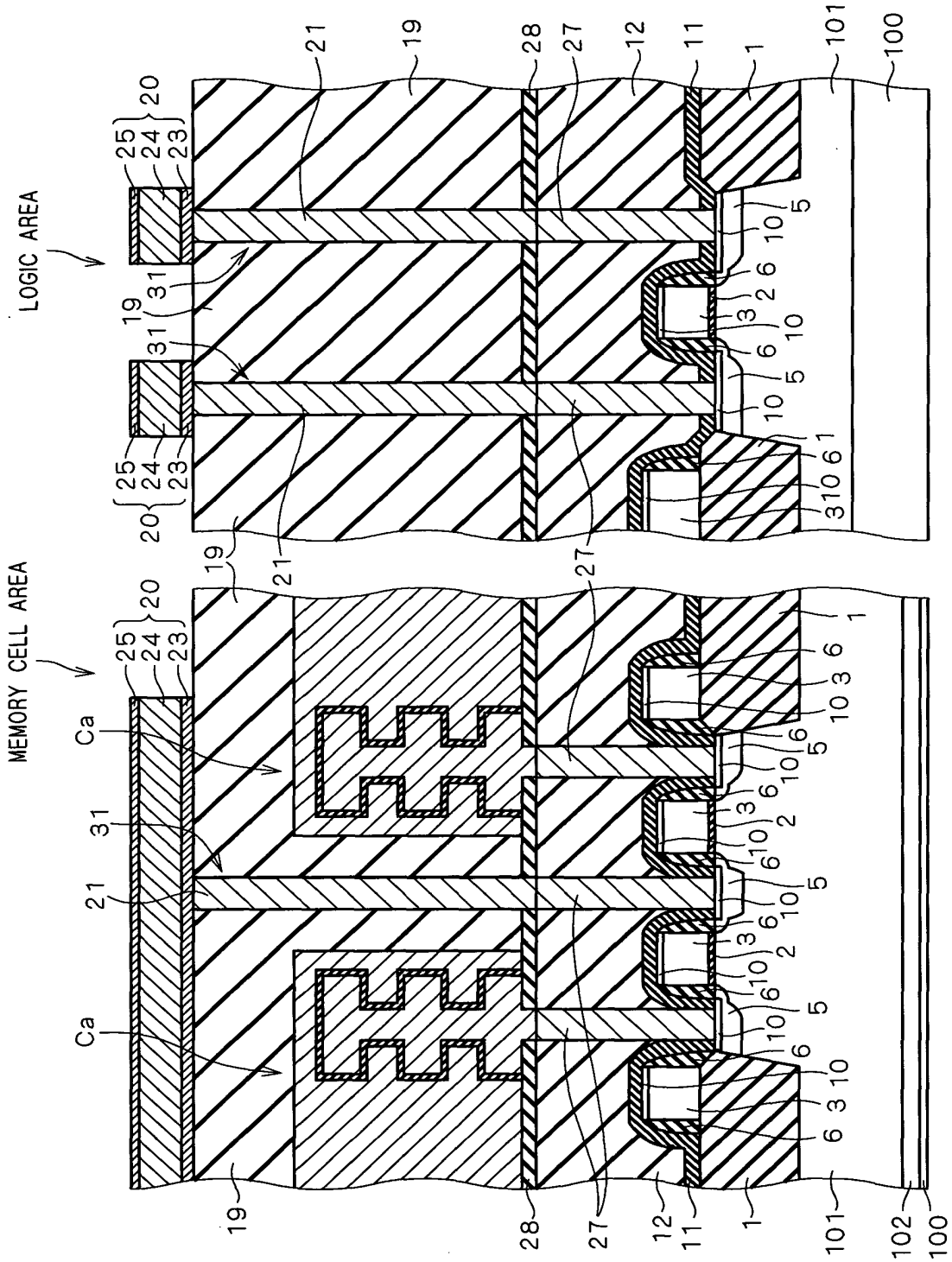
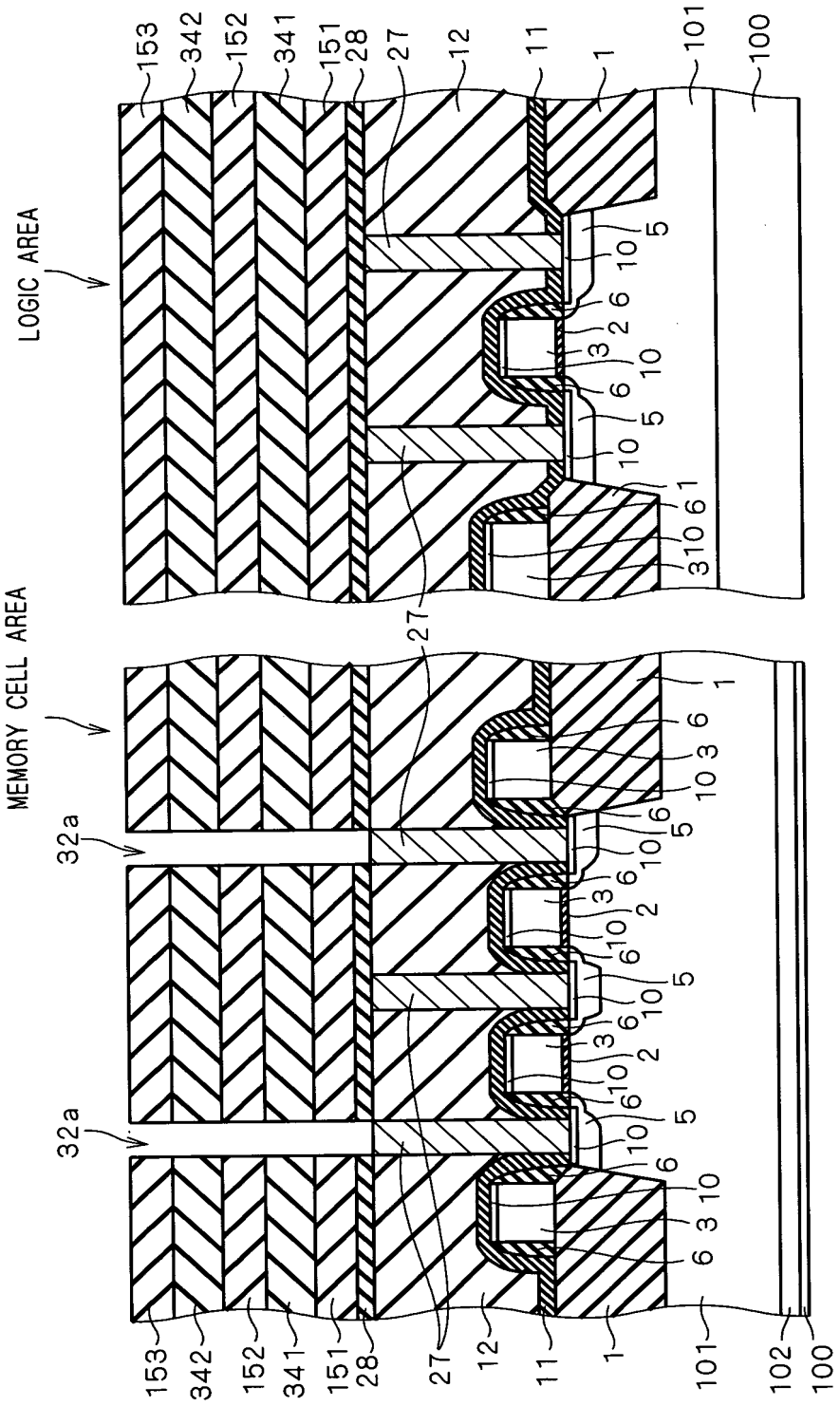

LOGIC AREA
MEMORY CELL AREA
Ca
Ca
19
21
27
28
12
11
1
101
102
100
20
23
24
25
31
10
6
5
3
2

FIG. 15


LOGIC AREA
MEMORY CELL AREA
32a
32a
153
342
152
341
151
28
27
12
11
1
101
102
100
5
10
6
2
3
10
6
5
10
6
1
10
3
1
6
3
10
6
5
10
6
10
3
6
2
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6
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10
3
6
2
10
6
5
10
6
3
10
6
3
1
27

FIG. 16

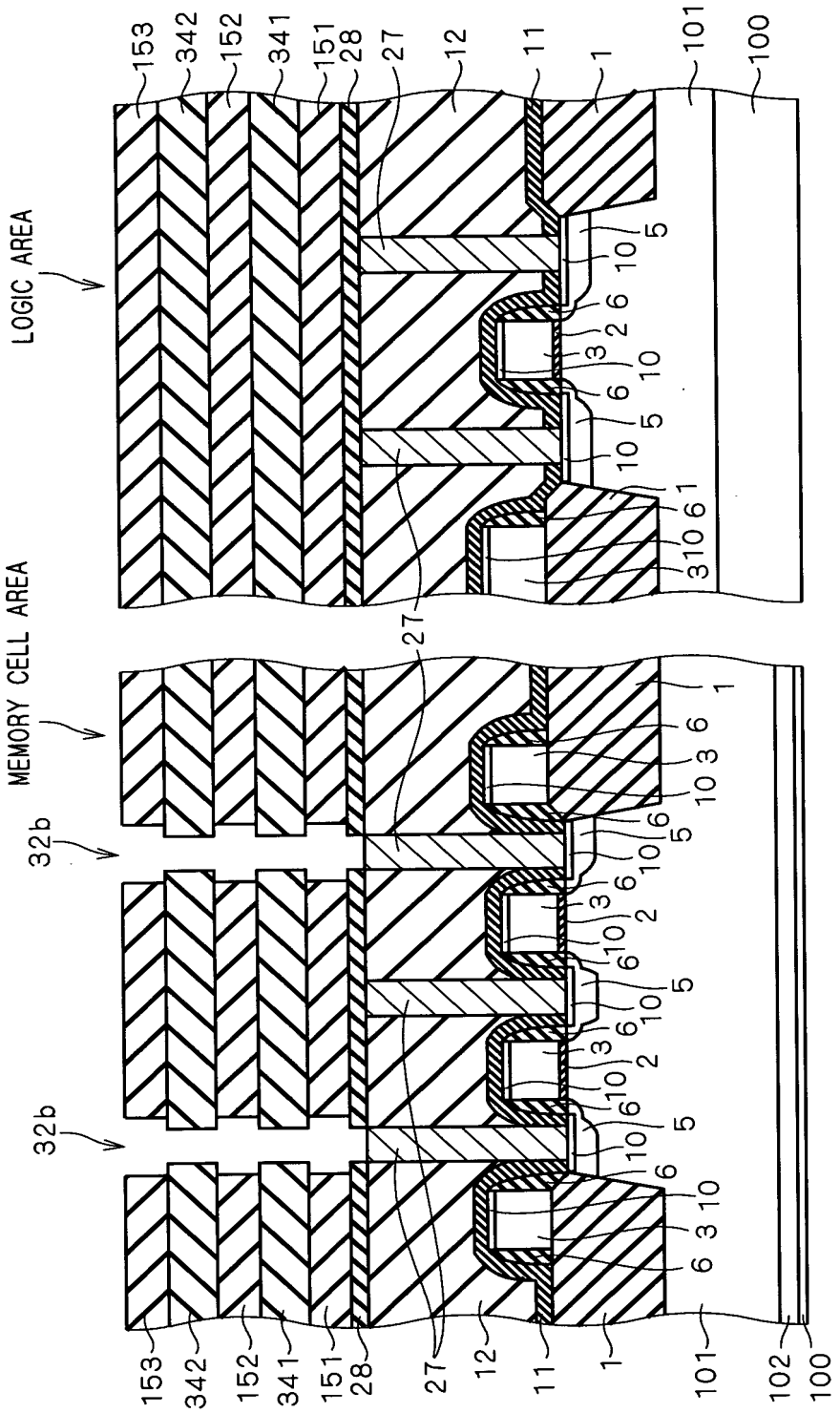

LOGIC AREA
MEMORY CELL AREA
32b
32b
153
342
152
341
151
28
27
12
11
1
101
102
100
5
10
6
2
3

FIG. 17

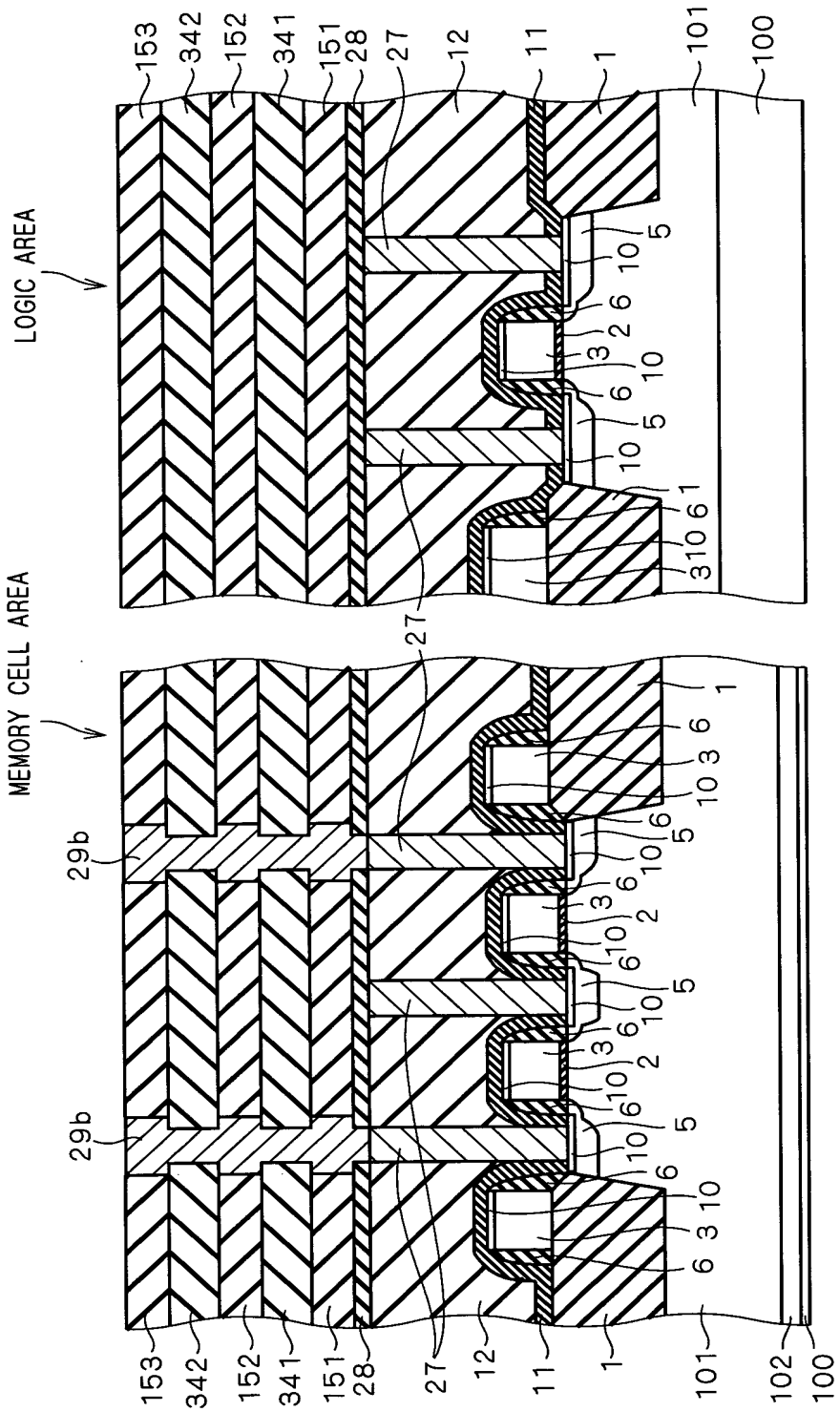

LOGIC AREA
MEMORY CELL AREA
153
342
152
341
151
28
27
12
11
1
101
100
102
29b
10
5
6
2
3

FIG. 18

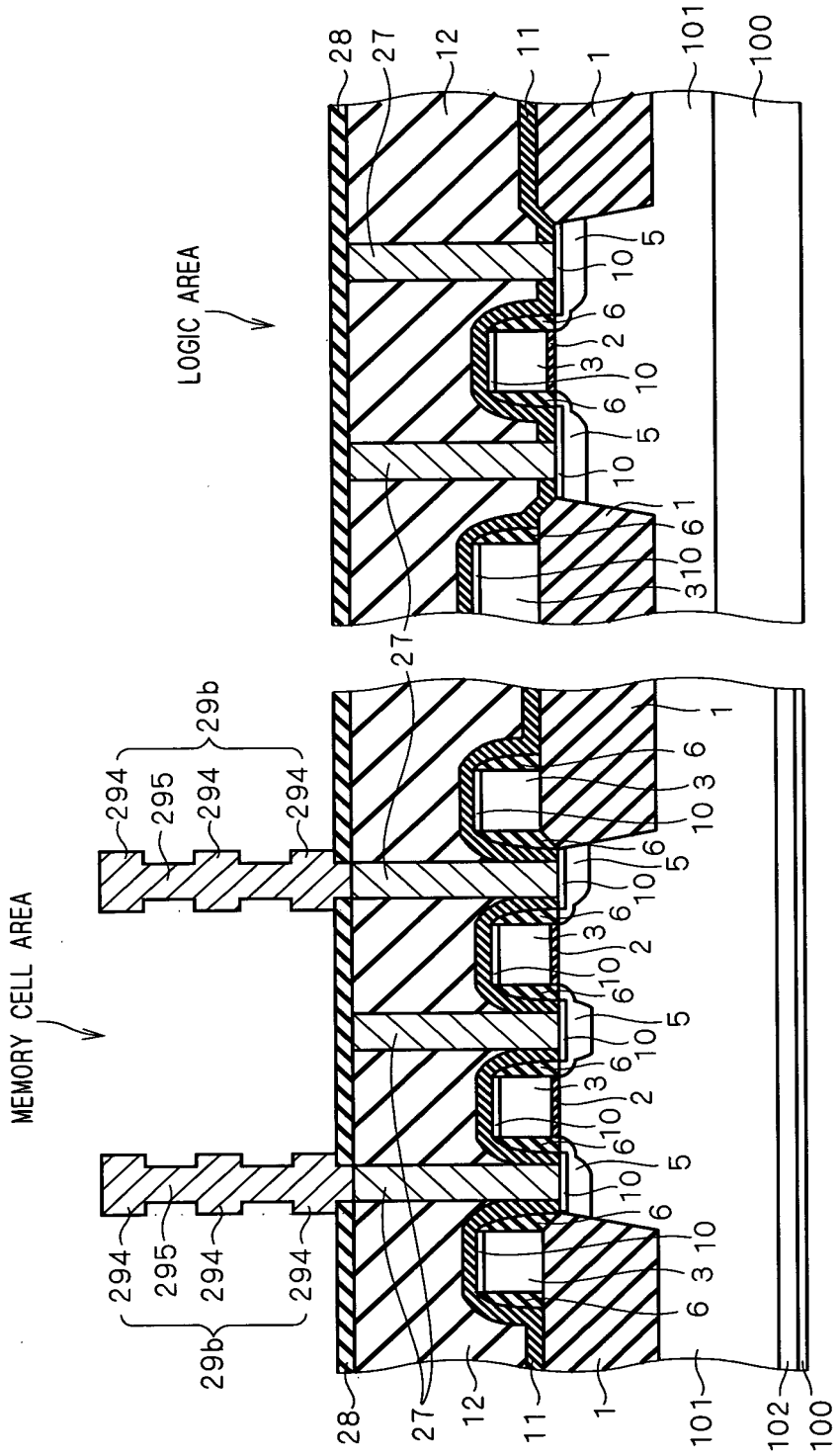
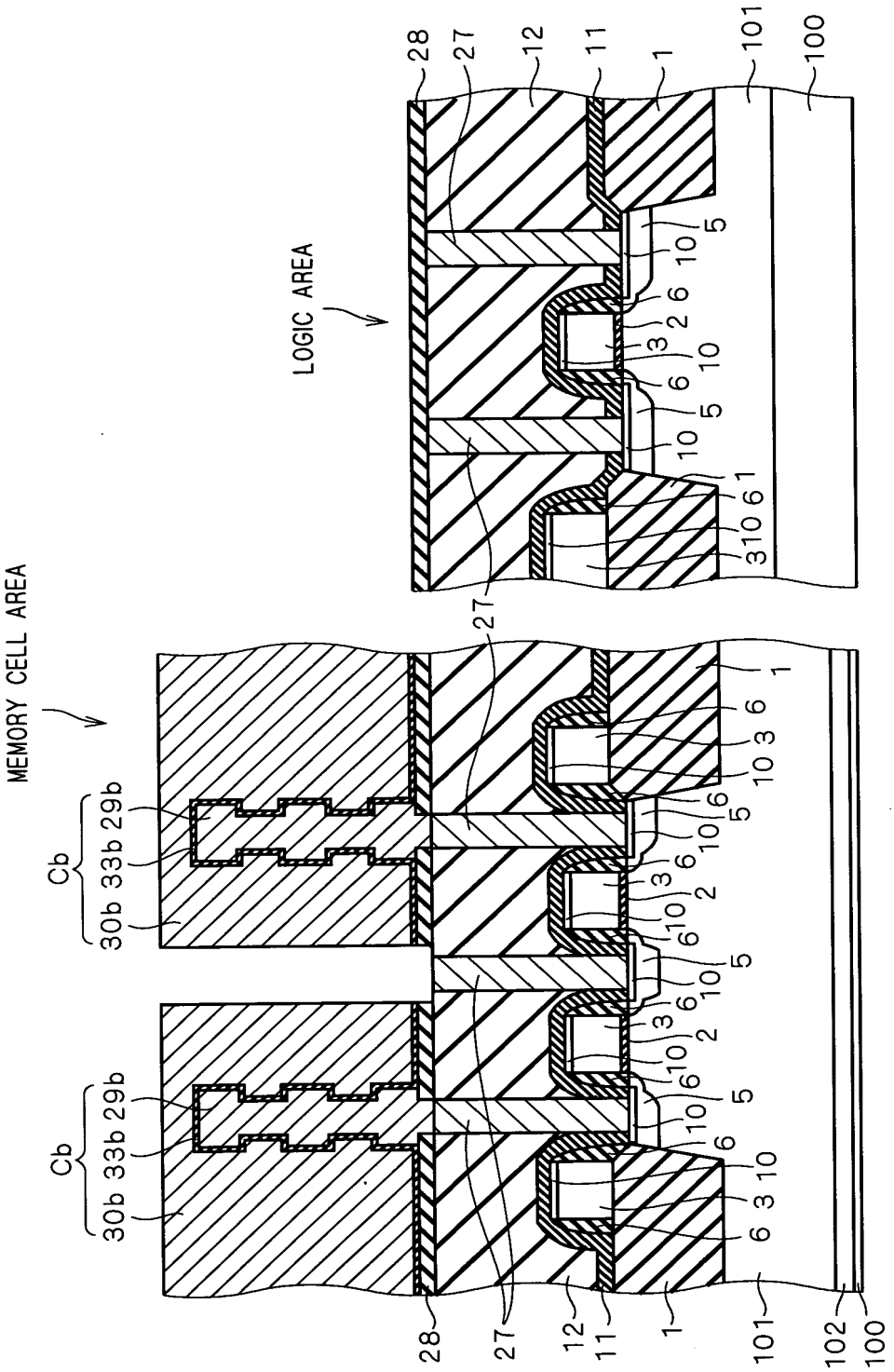

LOGIC AREA
MEMORY CELL AREA
28
27
12
11
1
101
100
102
29b
294
295
10
6
5
3
2

FIG. 19


MEMORY CELL AREA
LOGIC AREA
Cb
30b 33b 29b
28
27
12
11
1
101
100
102

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INV: Kouta INOUE, et al.
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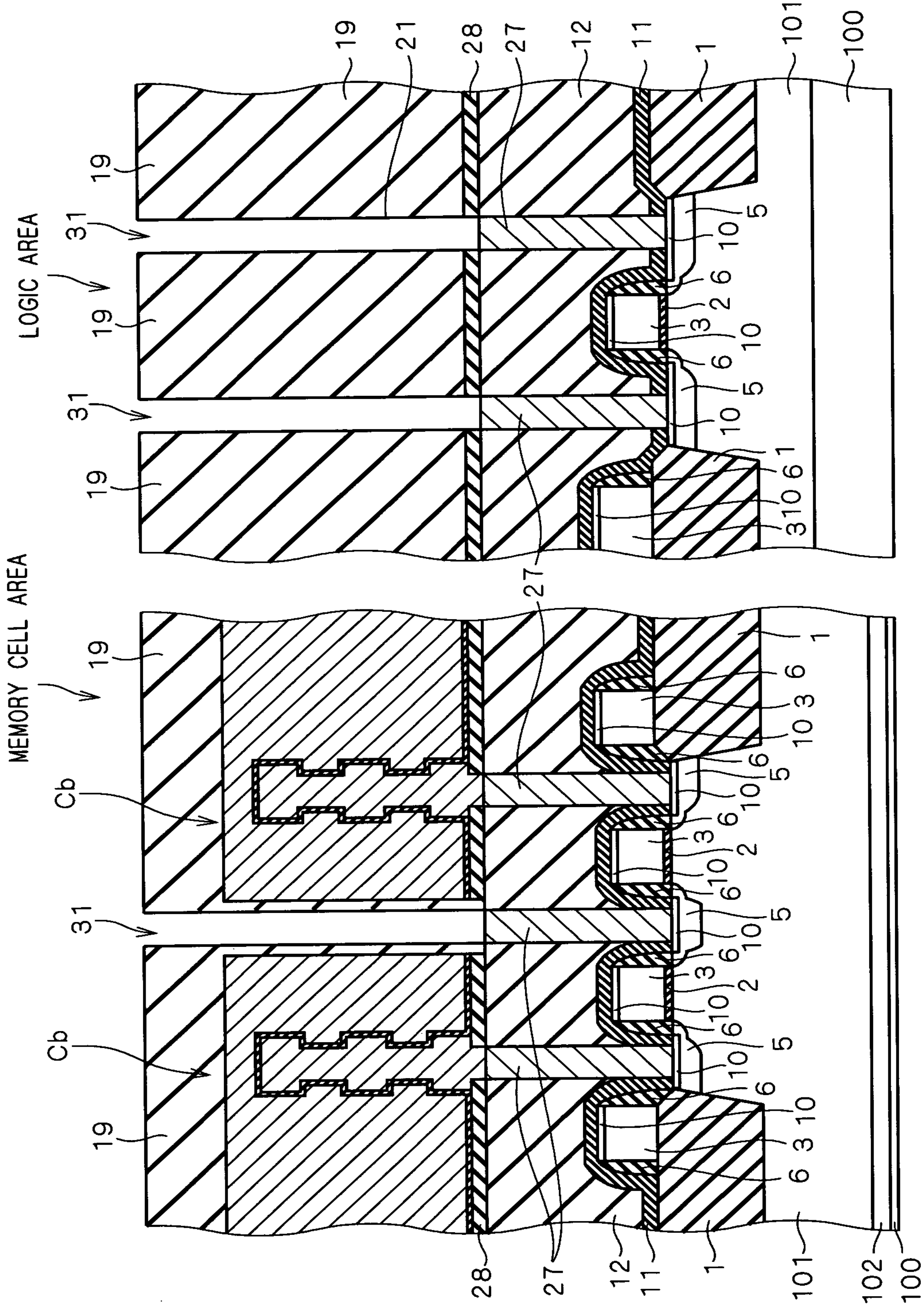


FIG. 21

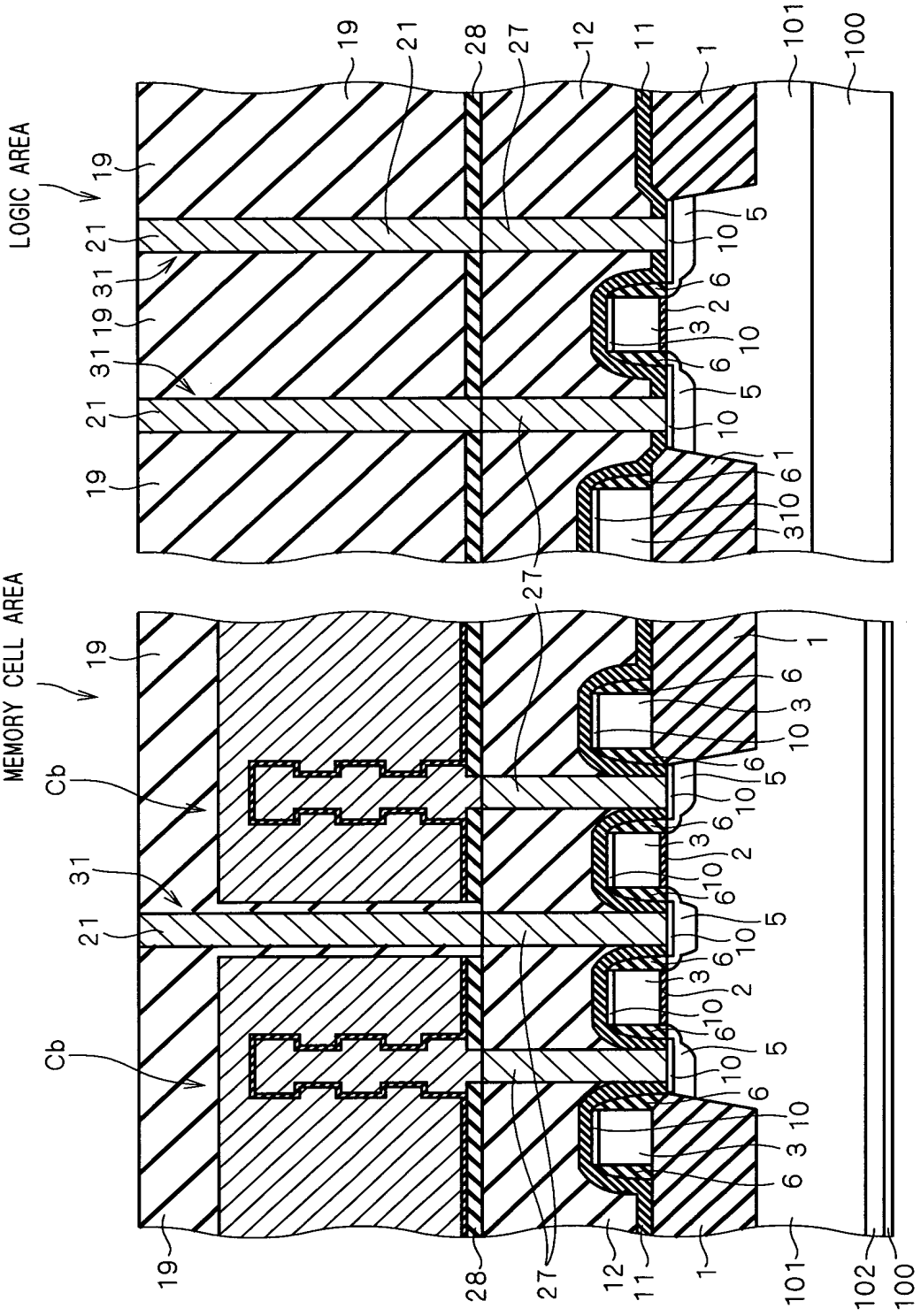

LOGIC AREA
MEMORY CELL AREA
Cb
Cb
19
21
28
27
12
11
1
101
100
102
31
5
10
6
3
2

FIG. 22

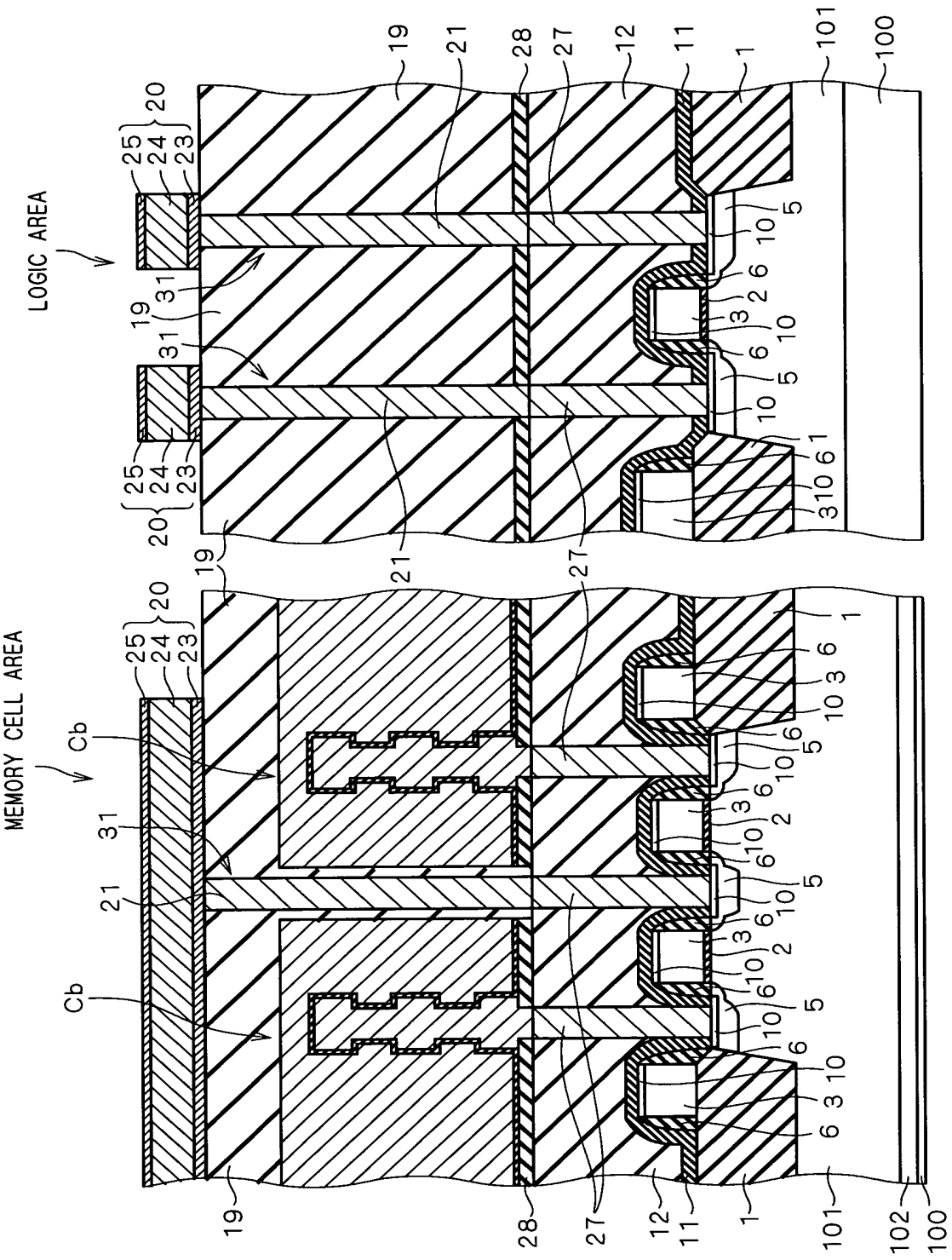

LOGIC AREA
MEMORY CELL AREA
Cb
Cb
19
21
28
27
12
11
1
101
100
102
20
25
24
23
31
5
10
6
2
3

FIG. 23

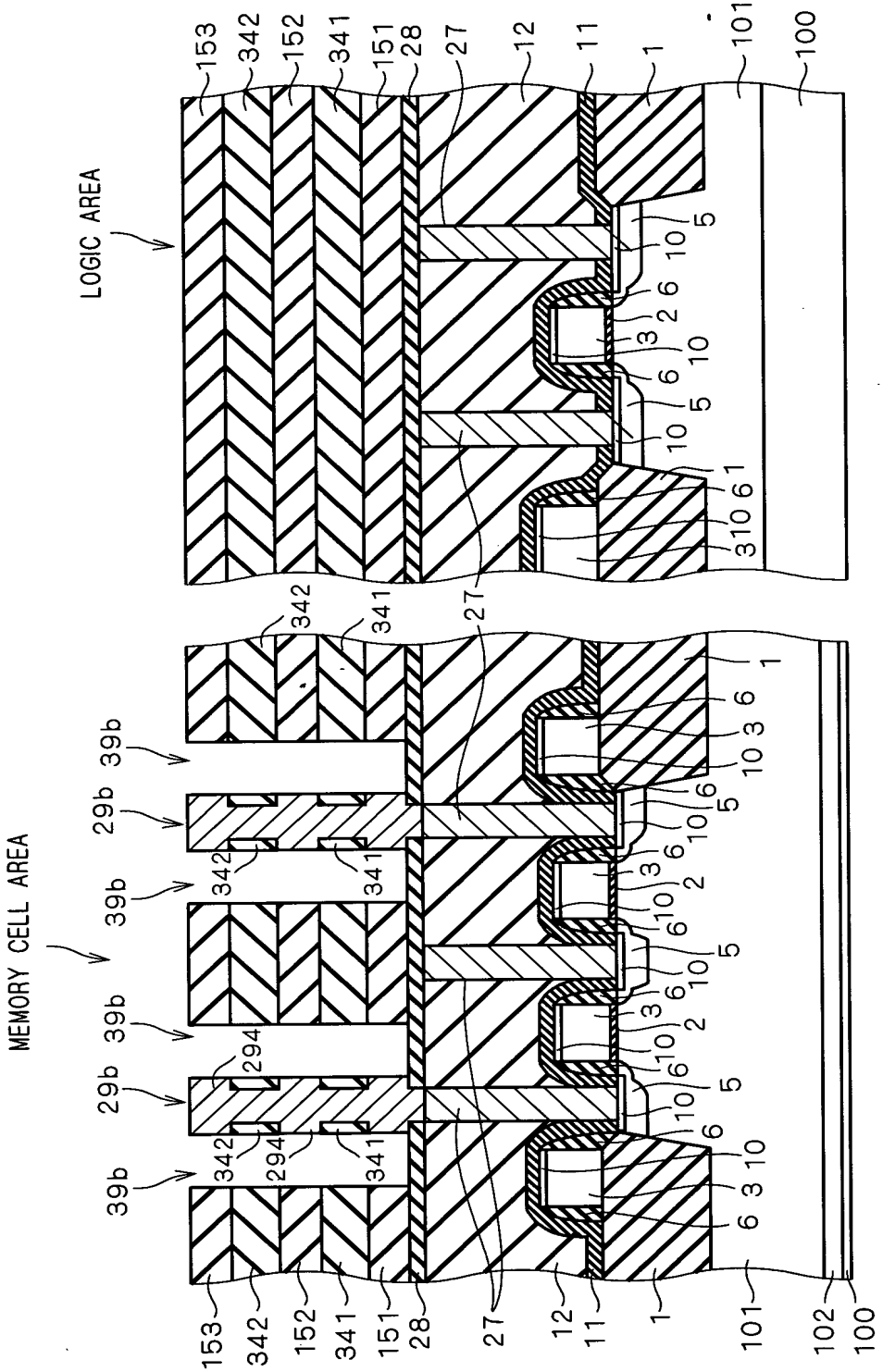

LOGIC AREA
MEMORY CELL AREA
153
342
152
341
151
28
27
12
11
1
101
100
102
39b
29b
294
10
6
5
3
2

FIG. 24

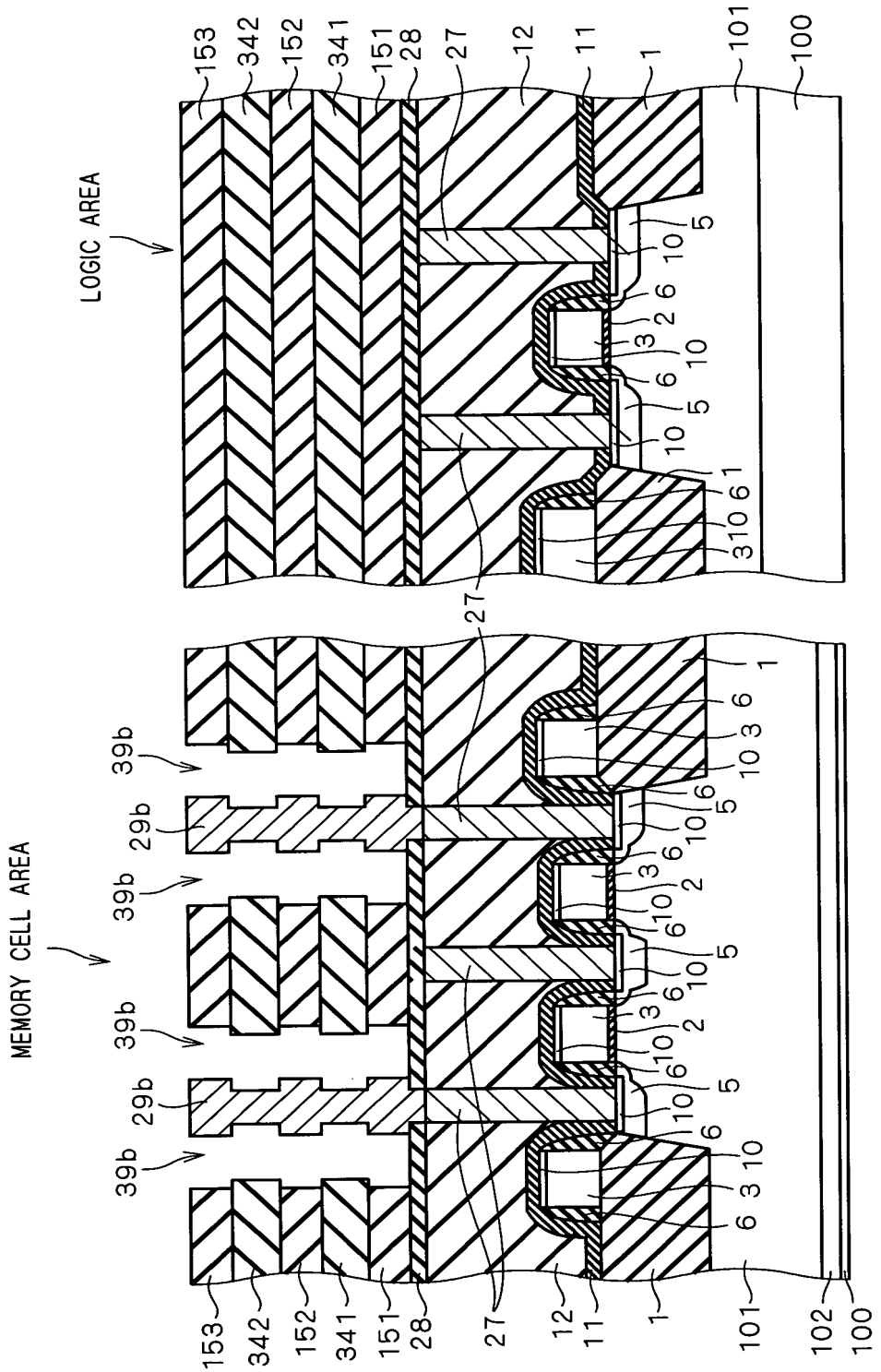

LOGIC AREA
MEMORY CELL AREA
153
342
152
341
151
28
27
12
11
1
101
100
102
39b
29b
10
6
5
3
2

FIG. 25

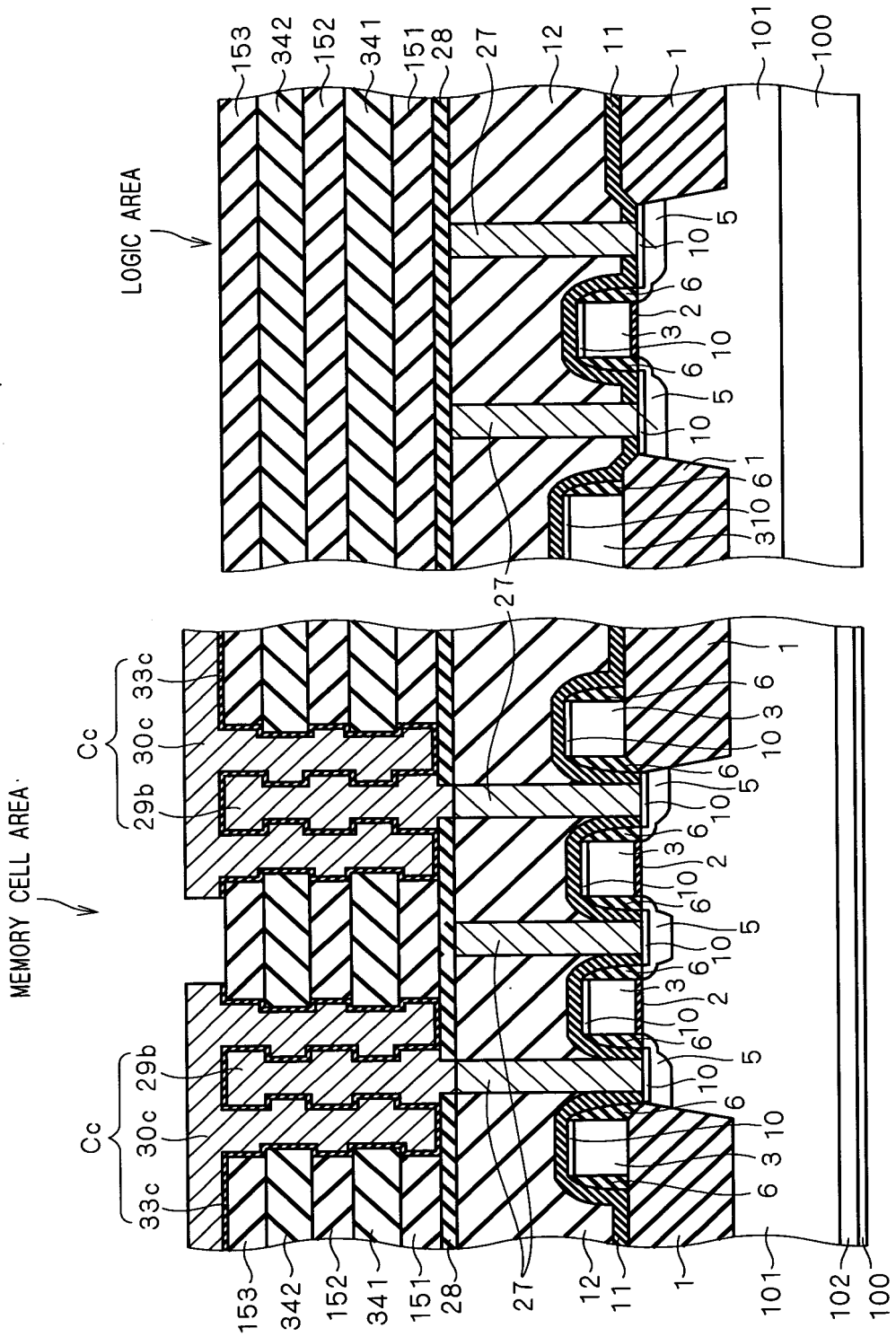

LOGIC AREA
MEMORY CELL AREA
Cc
153
342
152
341
151
28
27
12
11
1
101
100
102
29b
30c
33c
10
6
5
3
2

FIG. 26

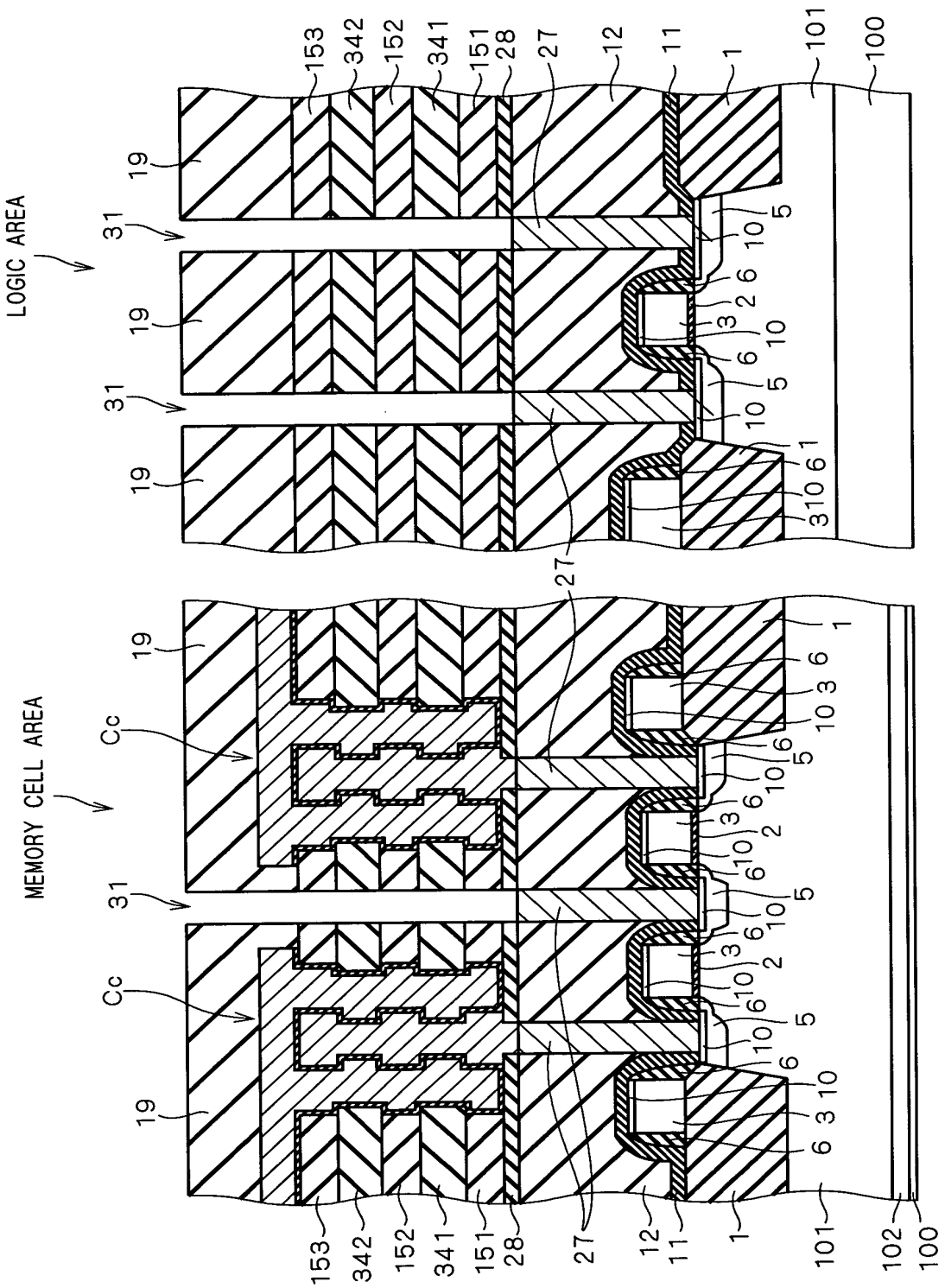

LOGIC AREA
MEMORY CELL AREA
Cc
Cc
153
342
152
341
151
28
27
12
11
1
101
102
100
19
31
5
10
6
3
2

FIG. 27

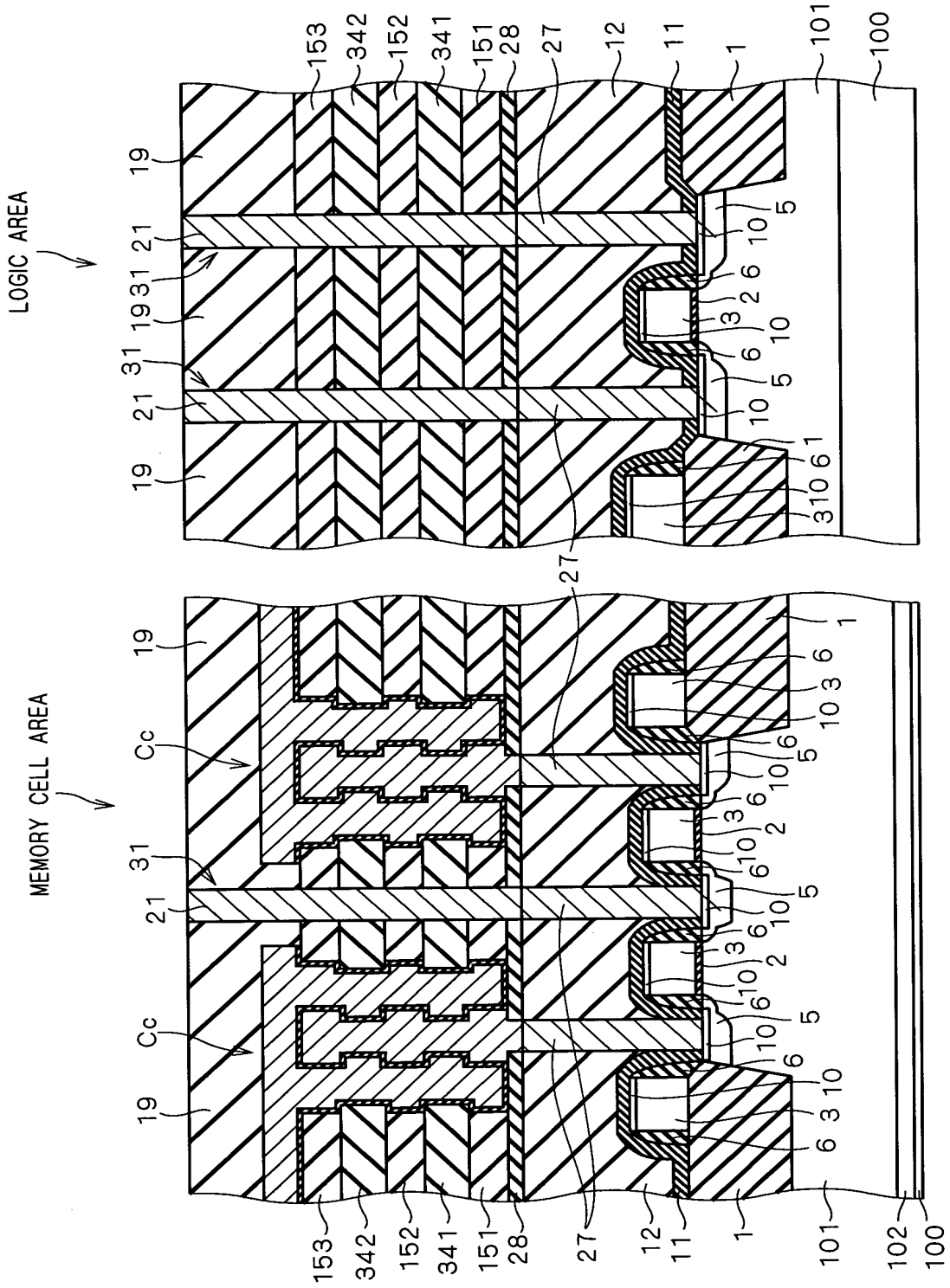

LOGIC AREA
MEMORY CELL AREA
Cc
Cc
153
342
152
341
151
28
27
12
11
1
101
102
100
19
21
31
10
6
5
3
2

FIG. 28

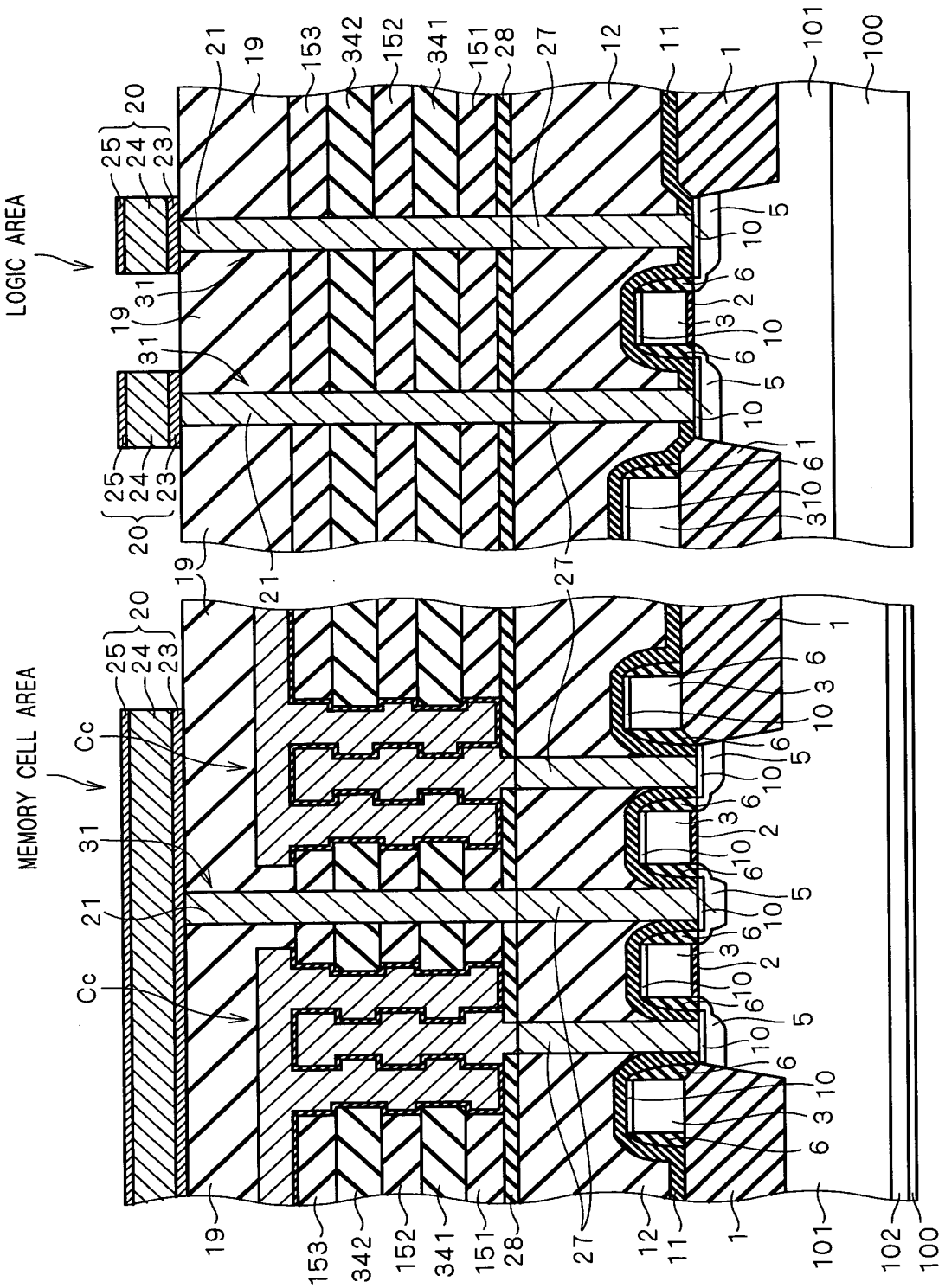

LOGIC AREA
MEMORY CELL AREA
Cc
Cc
Cc
20
25
24
23
31
21
19
153
342
152
341
151
28
27
12
11
1
101
100
102
5
10
6
3
2

FIG. 29

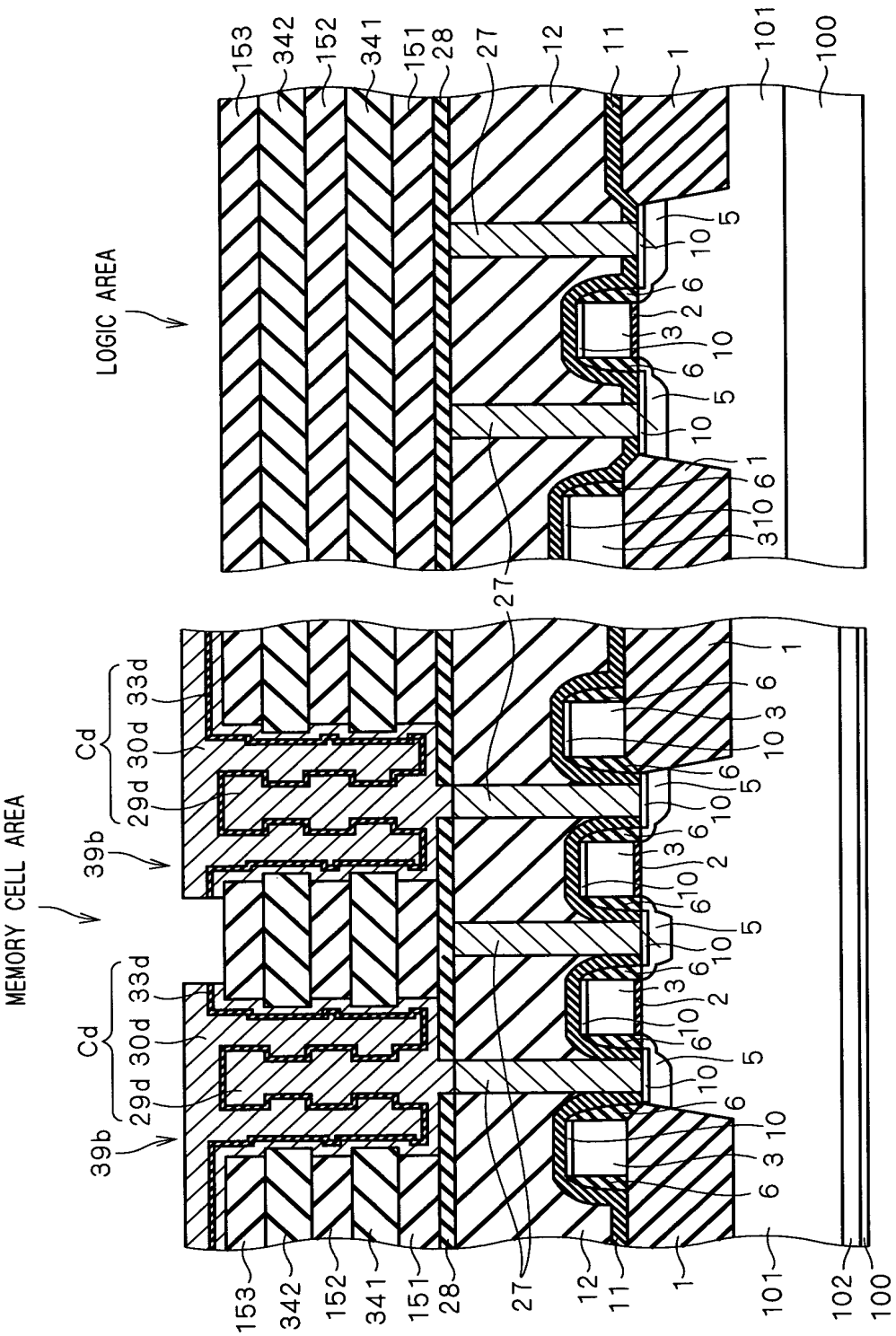

LOGIC AREA
MEMORY CELL AREA
153
342
152
341
151
28
27
12
11
1
101
100
102
39b
Cd
29d
30d
33d
10
6
5
3
2

FIG. 30

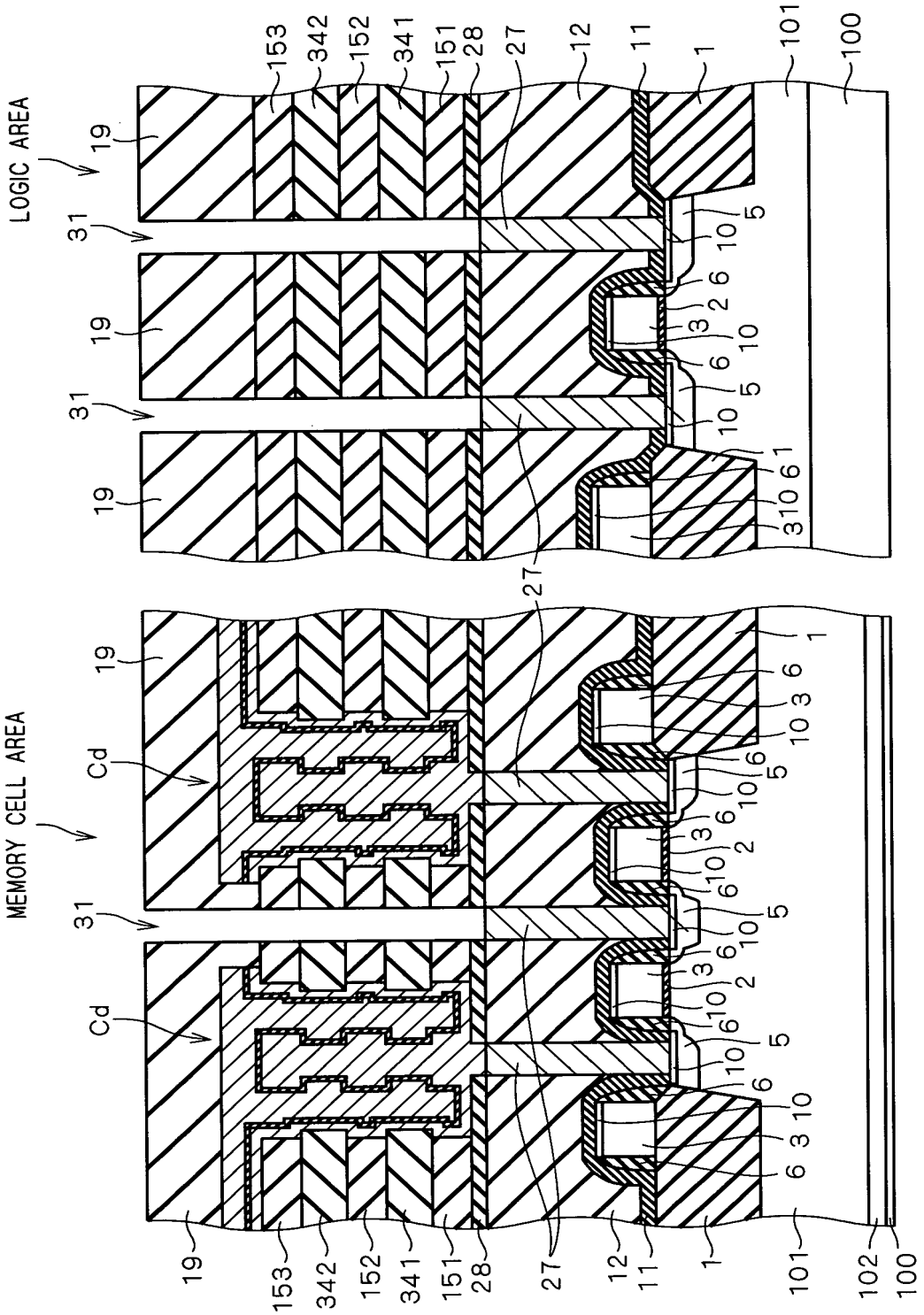

LOGIC AREA
MEMORY CELL AREA
19
31
Cd
153
342
152
341
151
28
27
12
11
1
101
102
100
2
3
5
6
10

FIG. 31

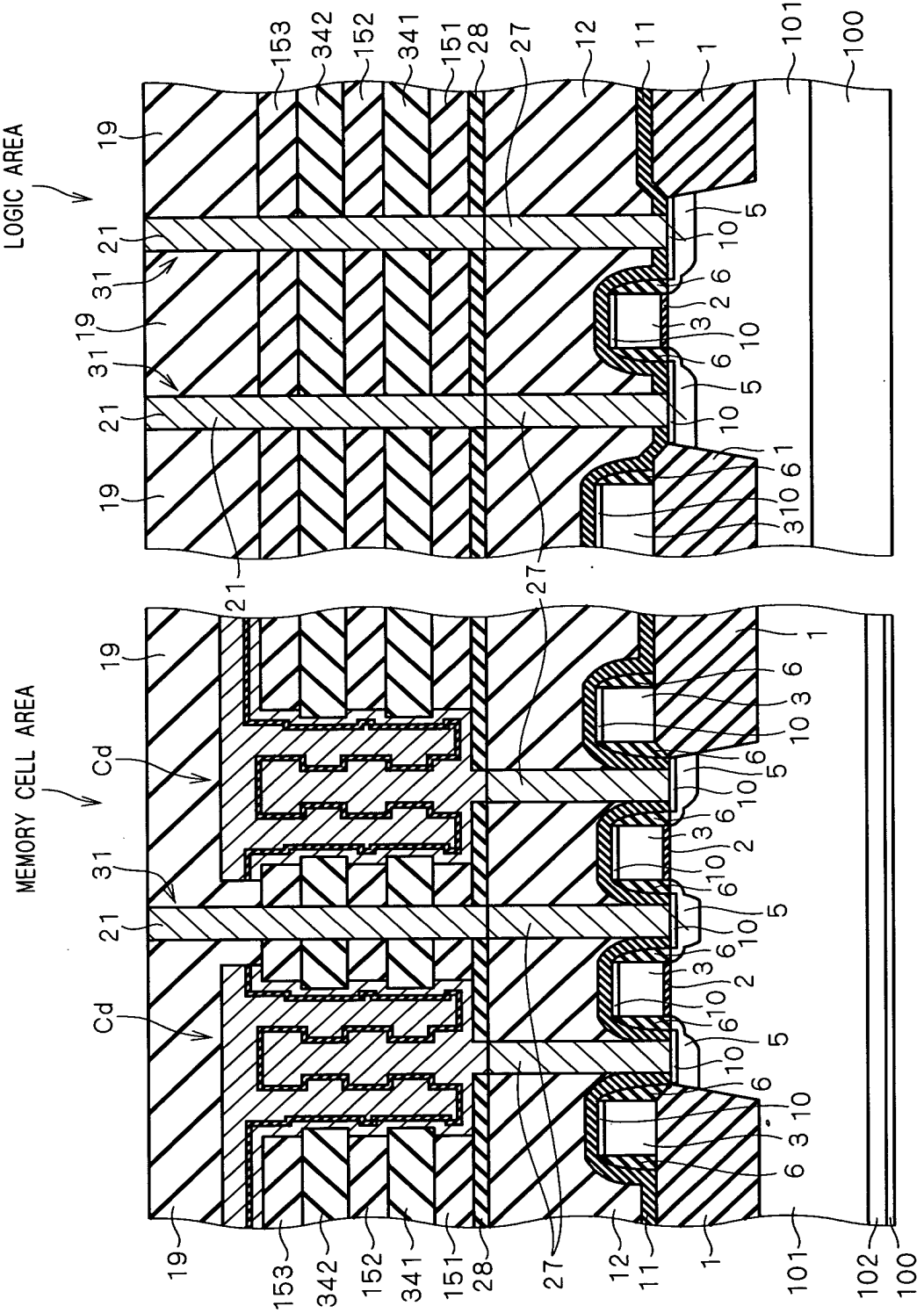

LOGIC AREA
MEMORY CELL AREA
Cd
19
21
31
153
342
152
341
151
28
27
12
11
1
101
100
102

FIG. 32

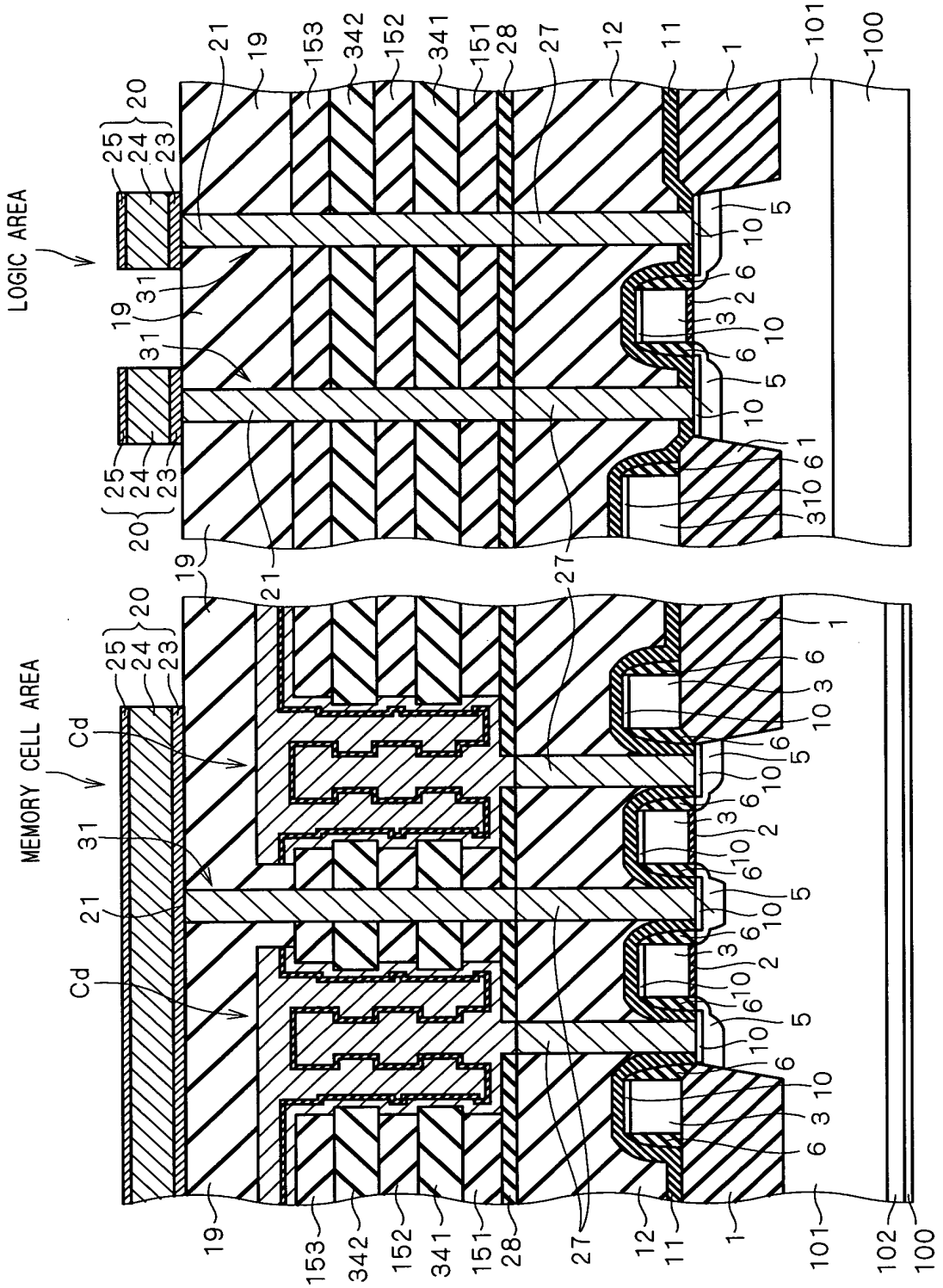

LOGIC AREA
MEMORY CELL AREA
Cd
Cd
19
153
342
152
341
151
28
27
12
11
1
101
102
100
20
25
24
23
31
21
10
6
5
3
2

FIG. 33

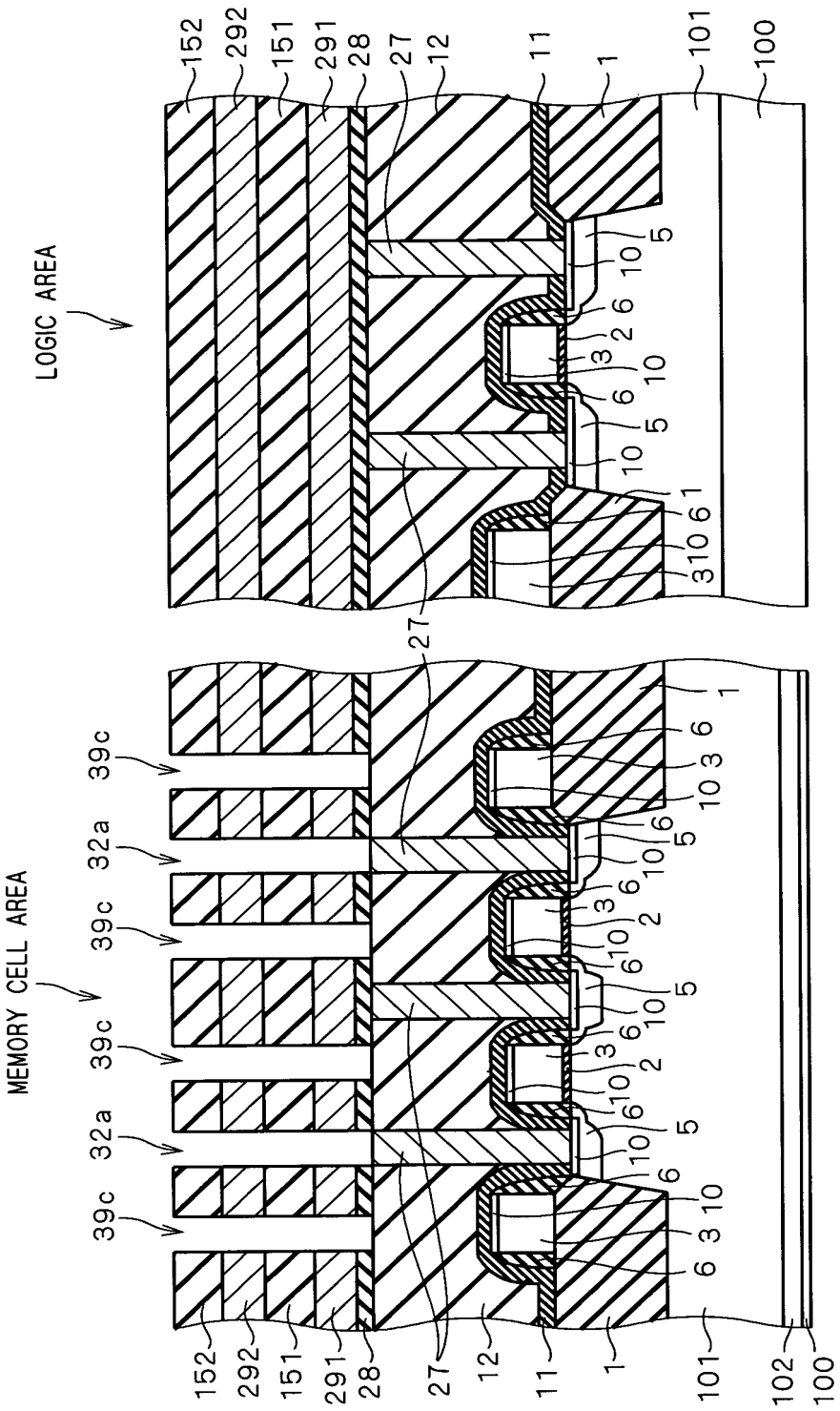

LOGIC AREA
MEMORY CELL AREA
152
292
151
291
28
27
12
11
1
101
100
102
39c
32a
5
10
6
3
2

FIG. 34

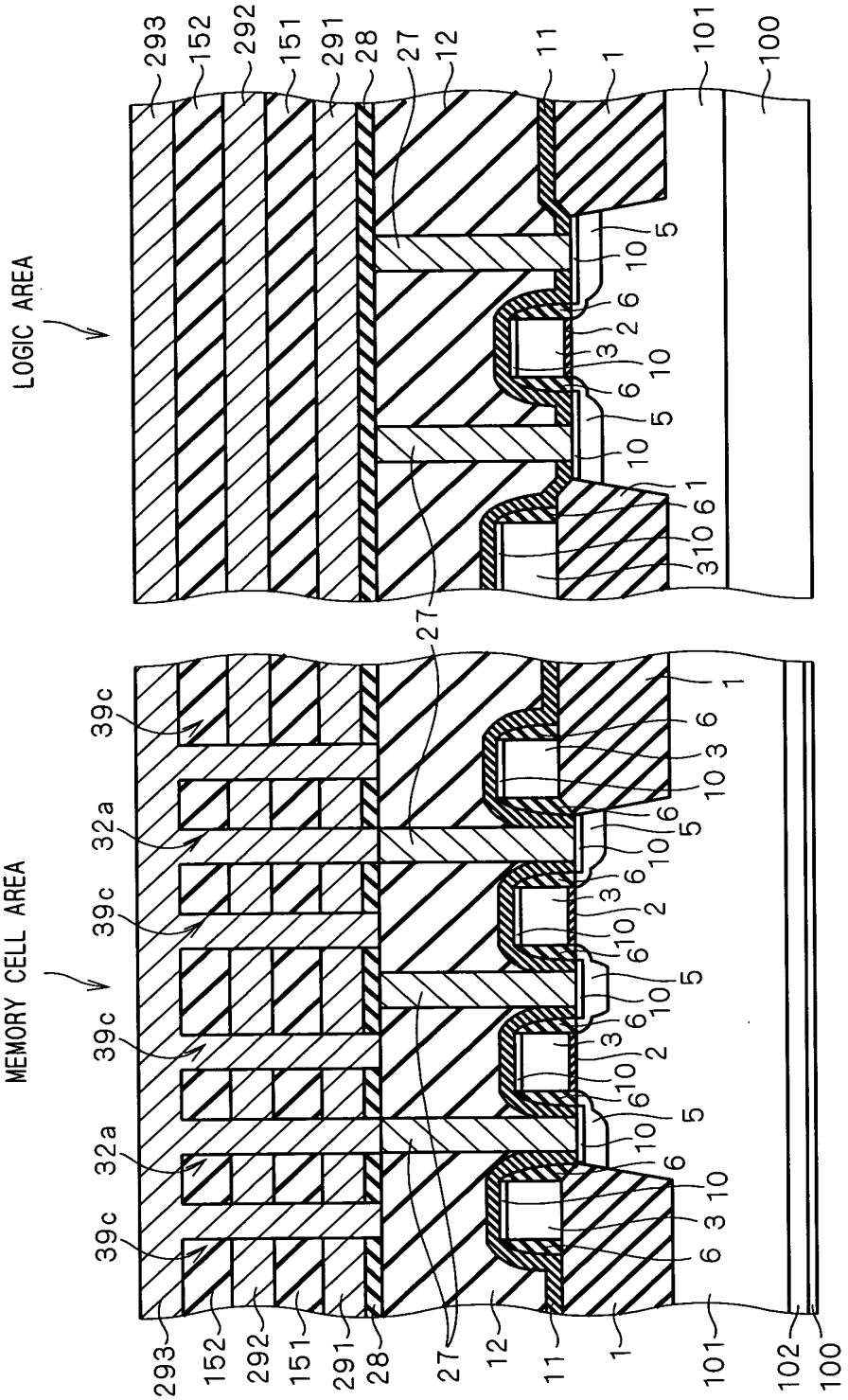

LOGIC AREA
MEMORY CELL AREA
293
152
292
151
291
28
27
12
11
1
101
100
102
39c
32a
5
10
6
3
2

FIG. 35

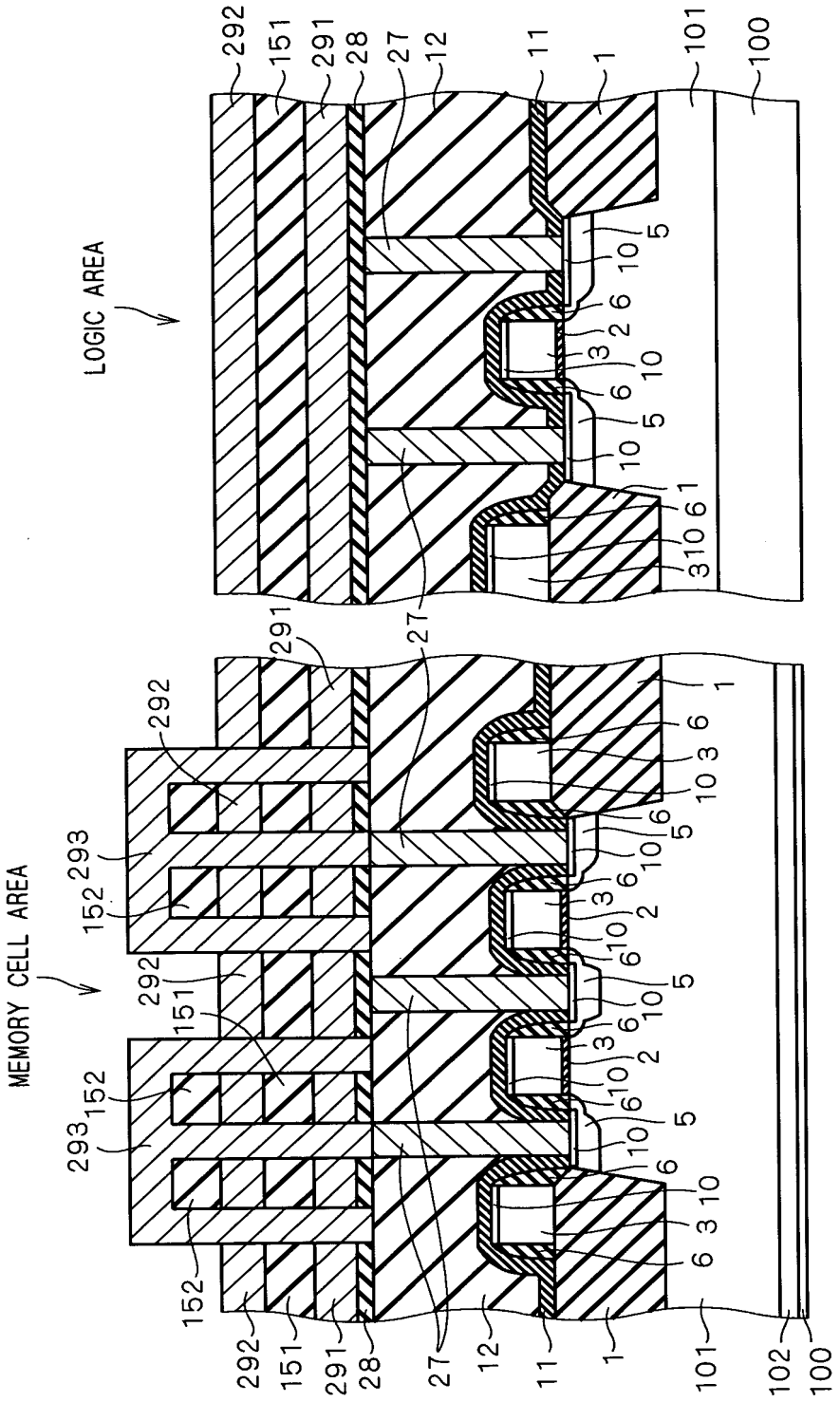

LOGIC AREA
MEMORY CELL AREA
292
151
291
28
27
12
11
1
101
100
102
293
152
10
6
5
3
2

FIG. 36

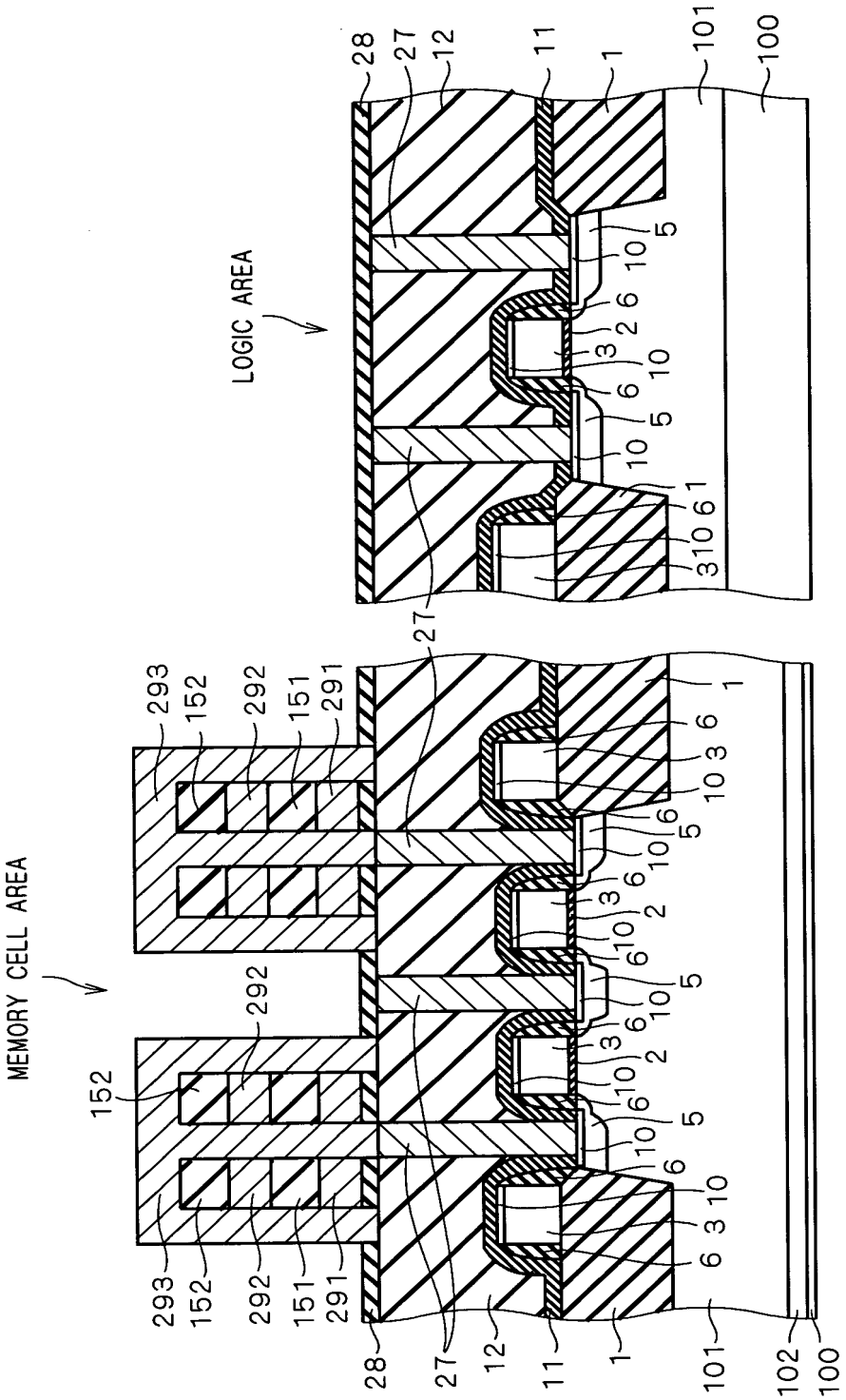

MEMORY CELL AREA
LOGIC AREA
293
152
292
151
291
28
27
12
11
1
101
102
100
10
6
5
3
2

FIG. 37

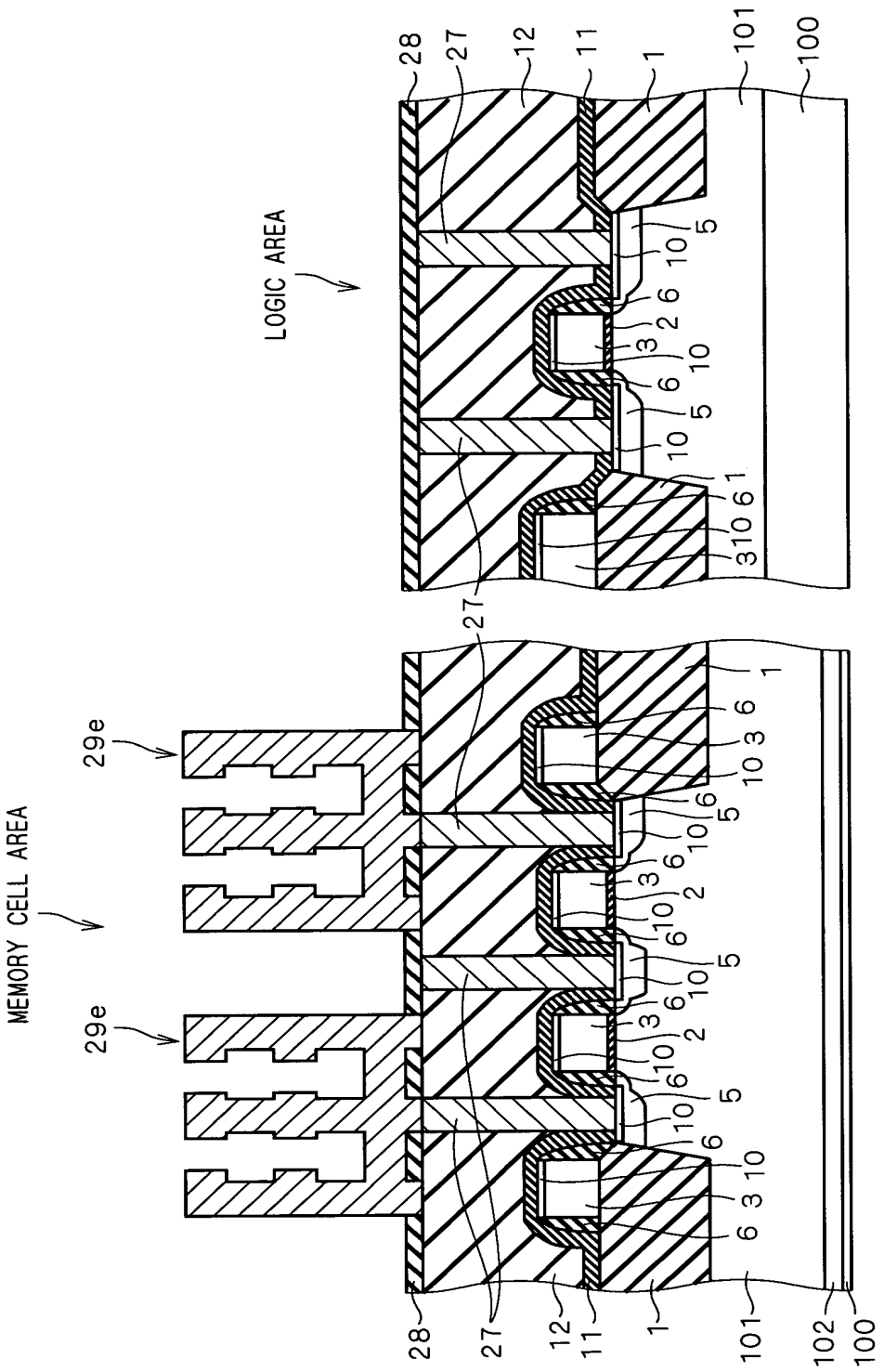


FIG. 38

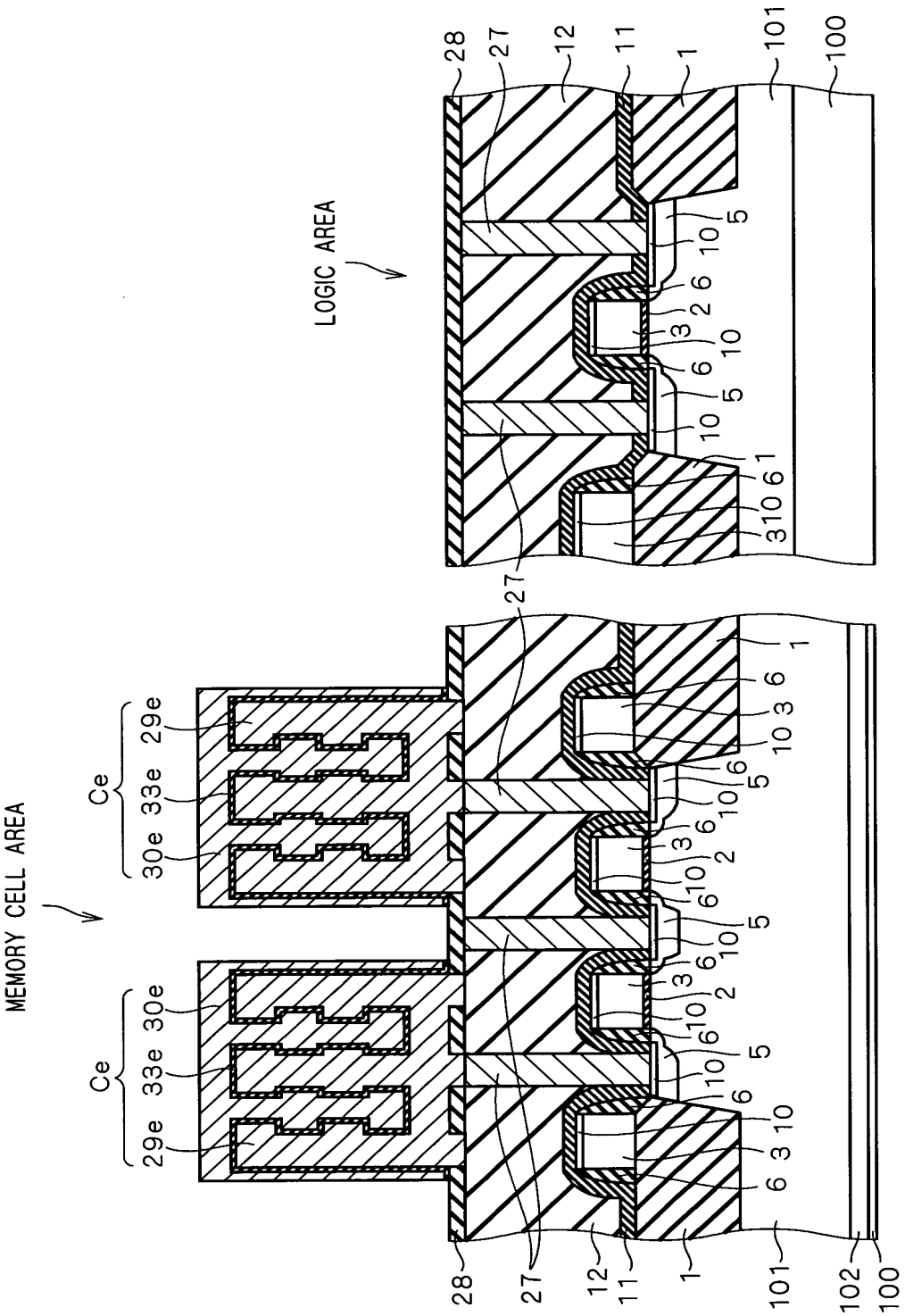
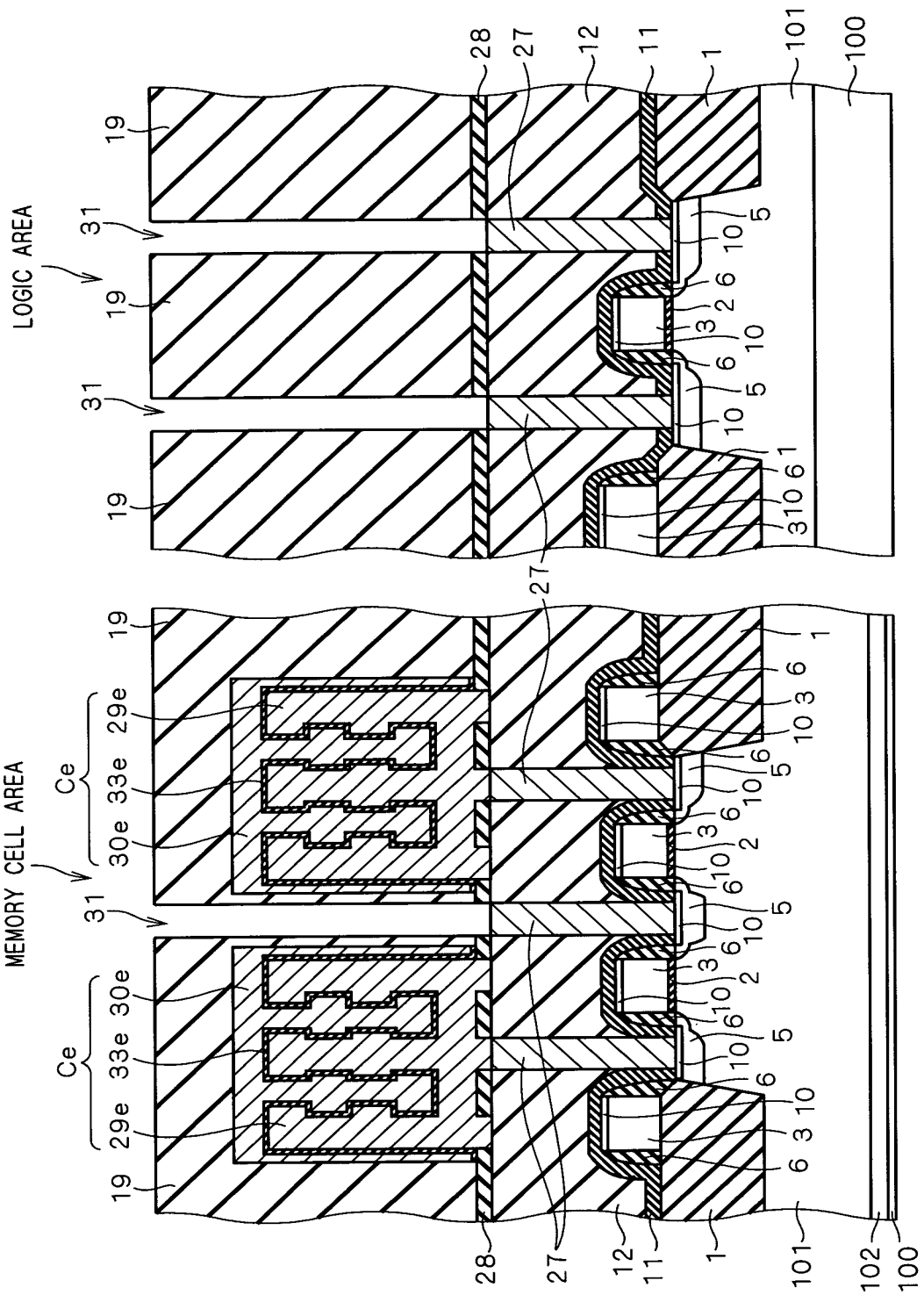
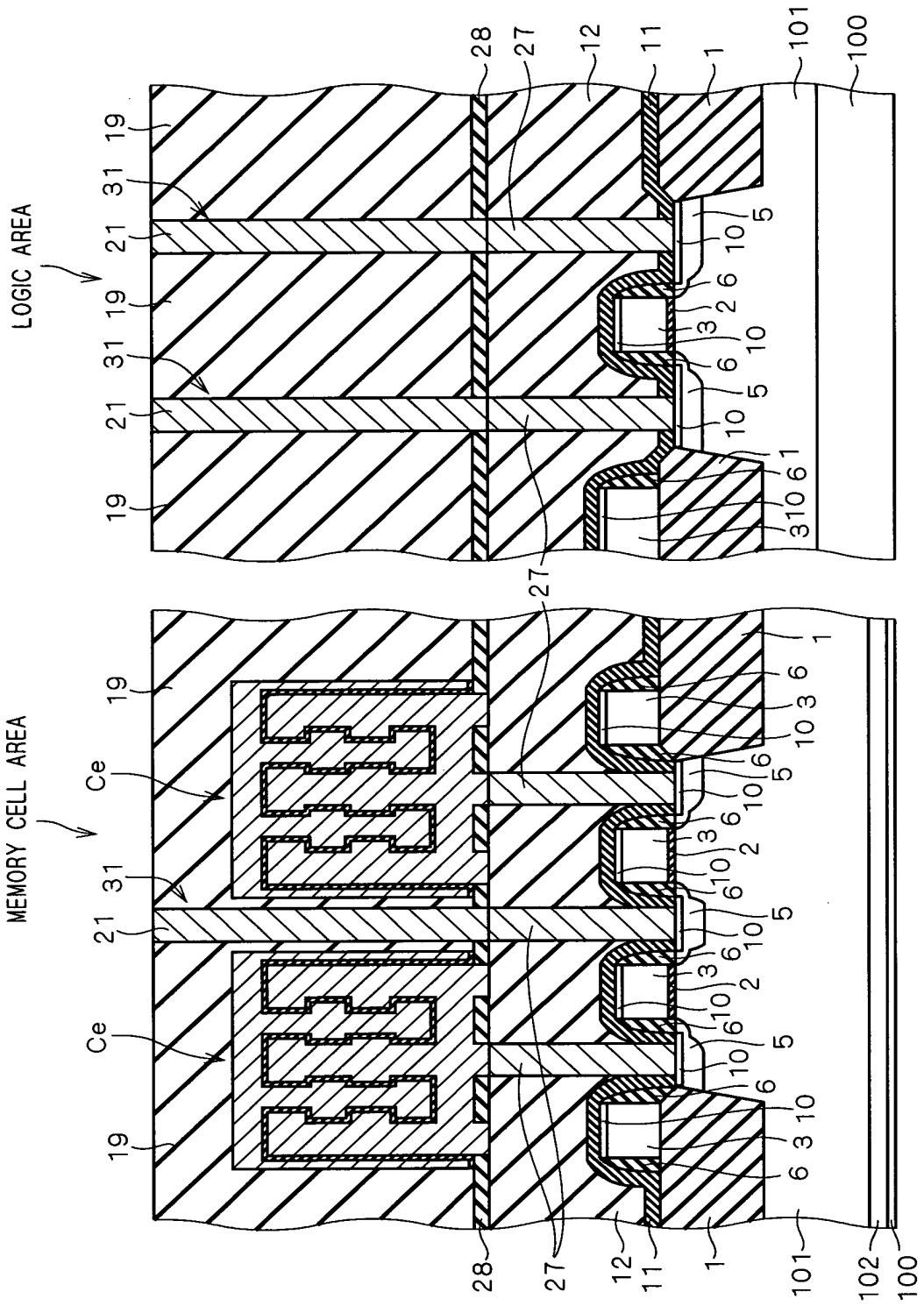

MEMORY CELL AREA
LOGIC AREA
Ce
Ce
29e
33e
30e
30e
33e
29e
28
27
12
11
1
101
100
102

FIG. 39


LOGIC AREA
MEMORY CELL AREA
Ce
19
31
29e
30e
33e
28
27
12
11
1
101
102
100
10
6
5
3
2

F I G . 4 0


LOGIC AREA
MEMORY CELL AREA
Ce
Ce
19
31
21
19
31
21
19
28
27
12
11
1
101
100
102
5
10
6
2
3
10
6
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3
10
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6
2
3
10
6
5
10
6
3
10
6
1
27
28
27
12
11
1
101
102
100

FIG. 41

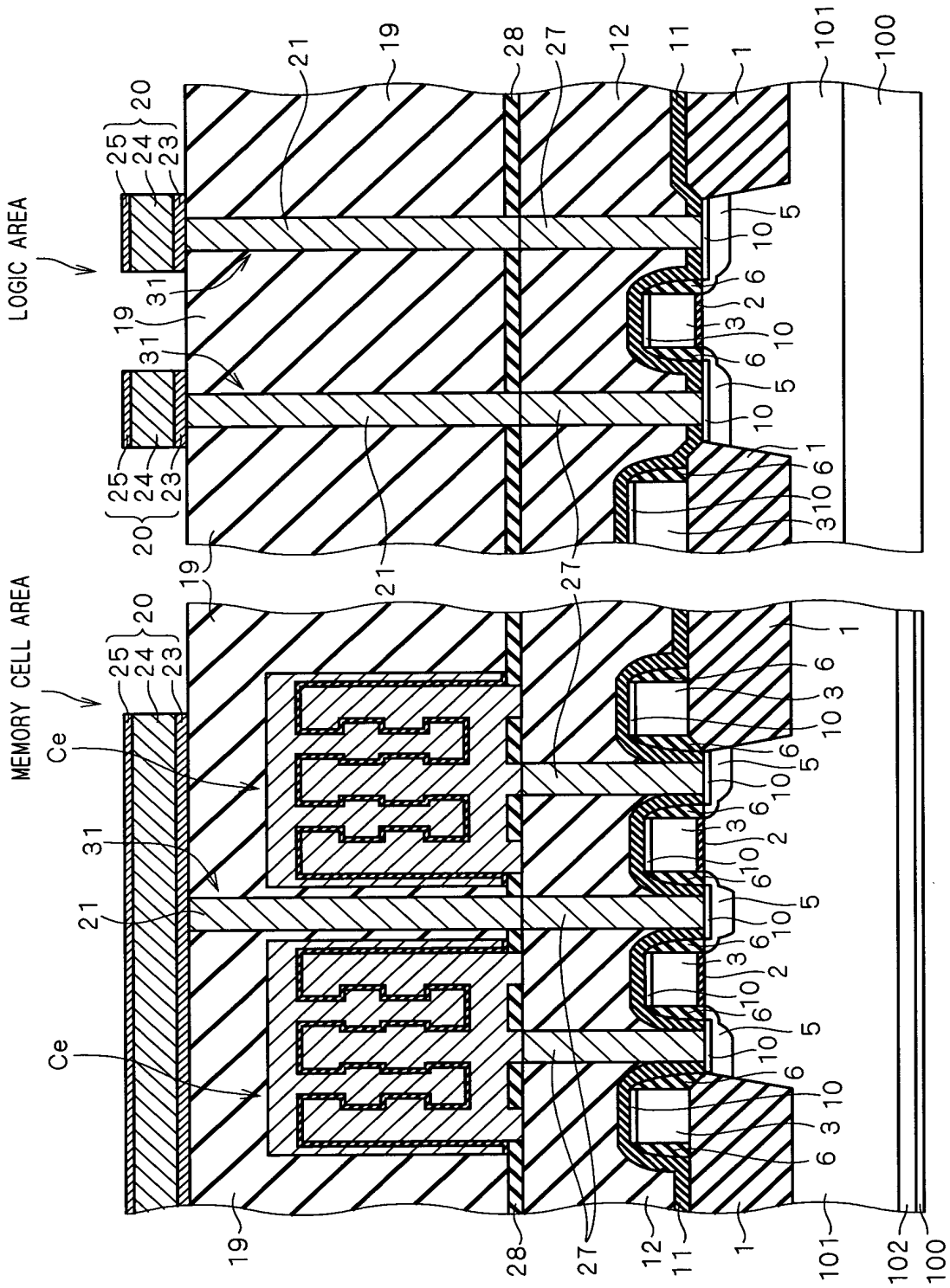

LOGIC AREA
MEMORY CELL AREA
Ce
Ce
19
21
28
27
12
11
1
101
102
100
20
25
24
23
31
10
6
5
3
2

FIG. 42

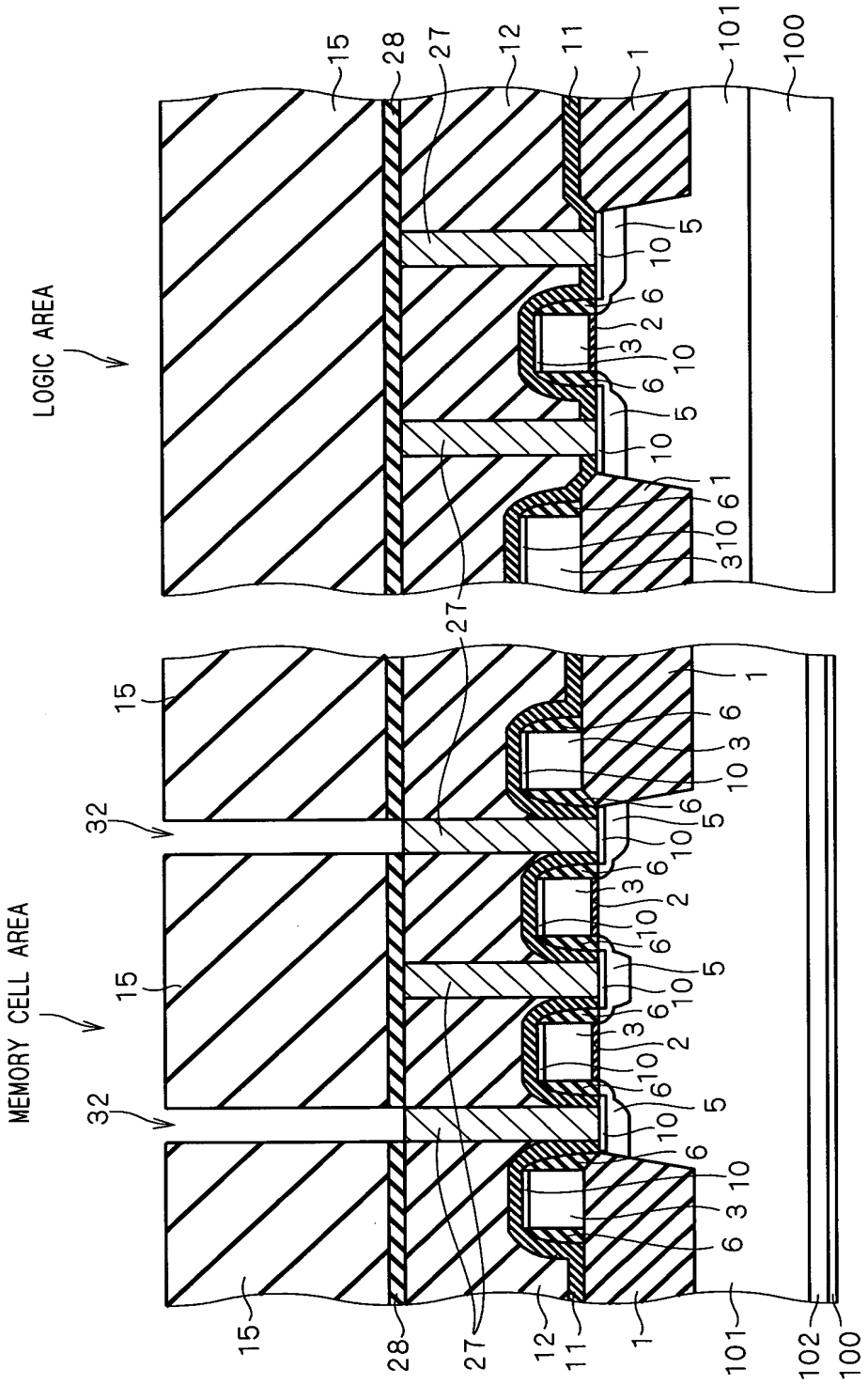

LOGIC AREA
MEMORY CELL AREA
15
28
27
12
11
1
101
100
102
32
5
10
6
2
3

FIG. 43

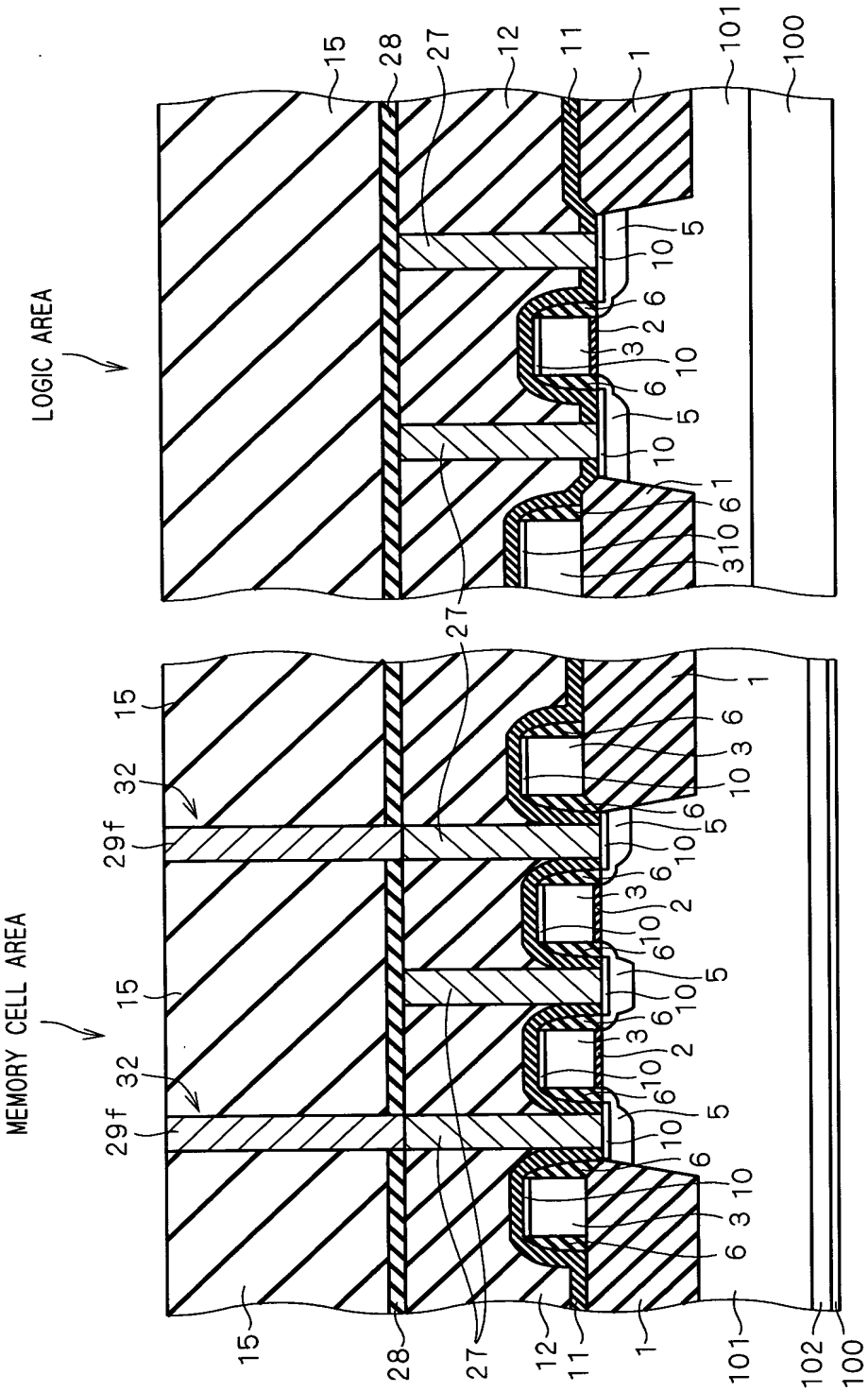


FIG. 44

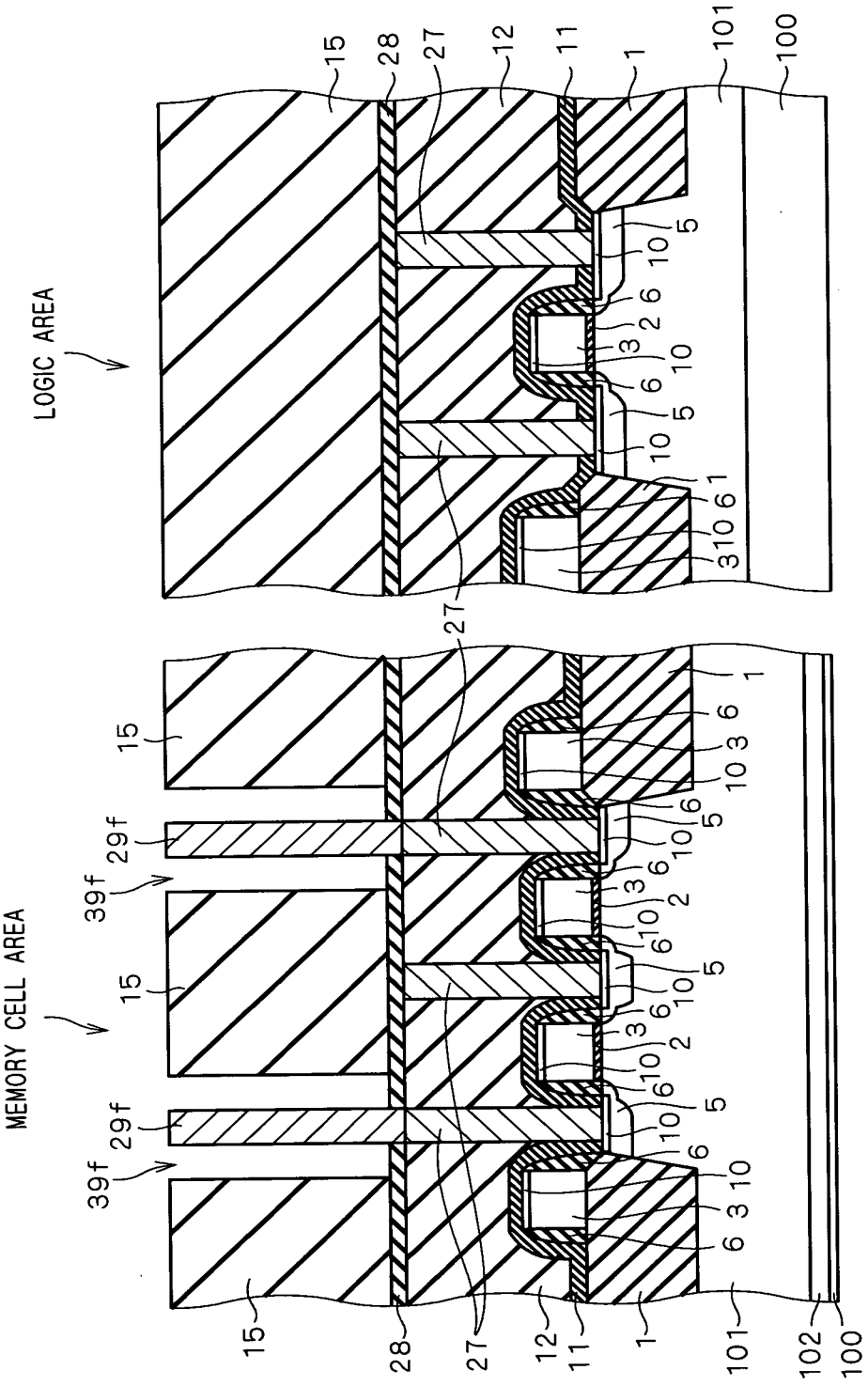

LOGIC AREA
MEMORY CELL AREA
15
28
27
12
11
1
101
100
102
29f
39f
10
6
5
3
2

FIG. 45

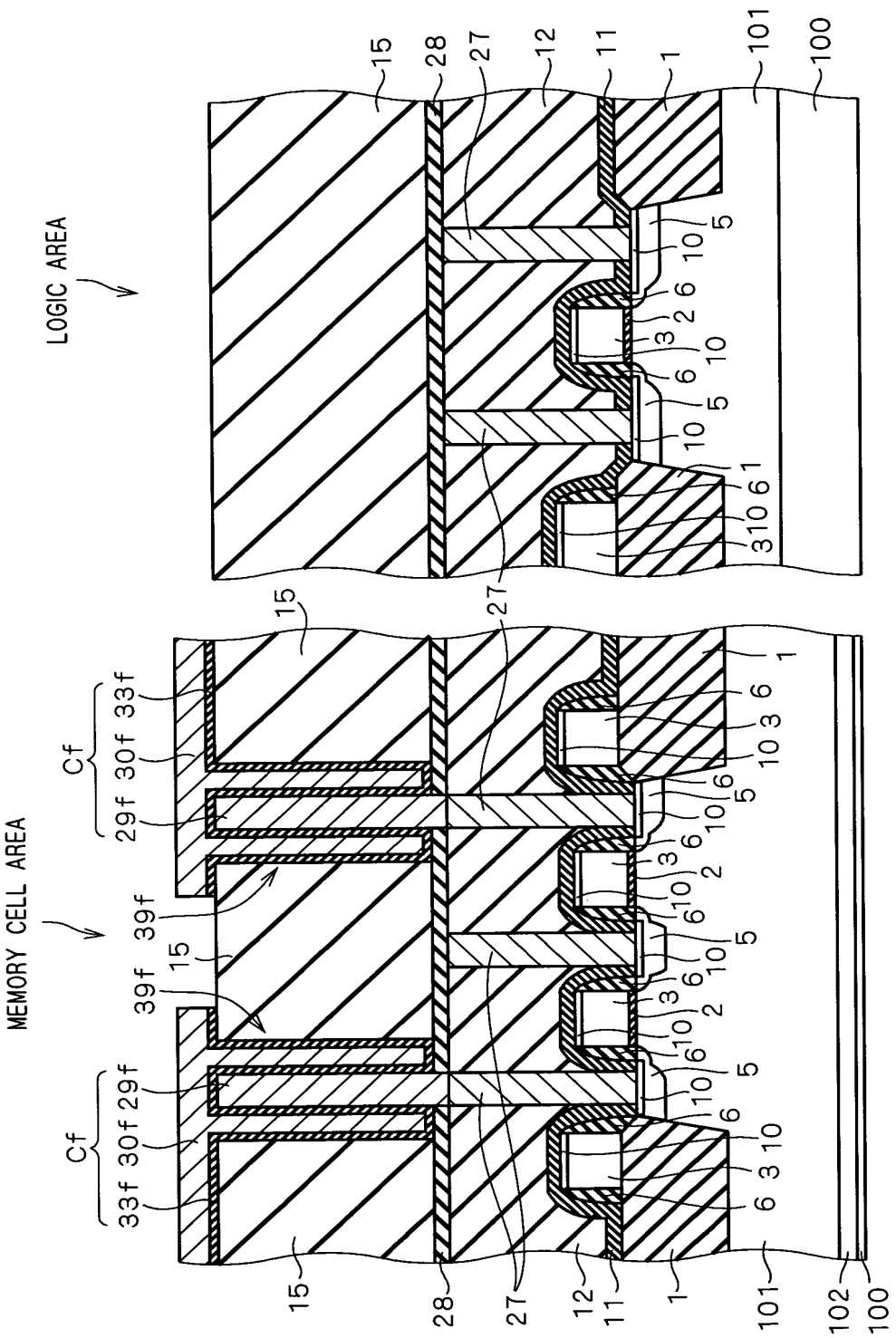

LOGIC AREA
MEMORY CELL AREA
Cf
15
28
27
12
11
1
101
100
102
5
10
6
2
3
61
310
29f
30f
33f
39f

FIG. 46

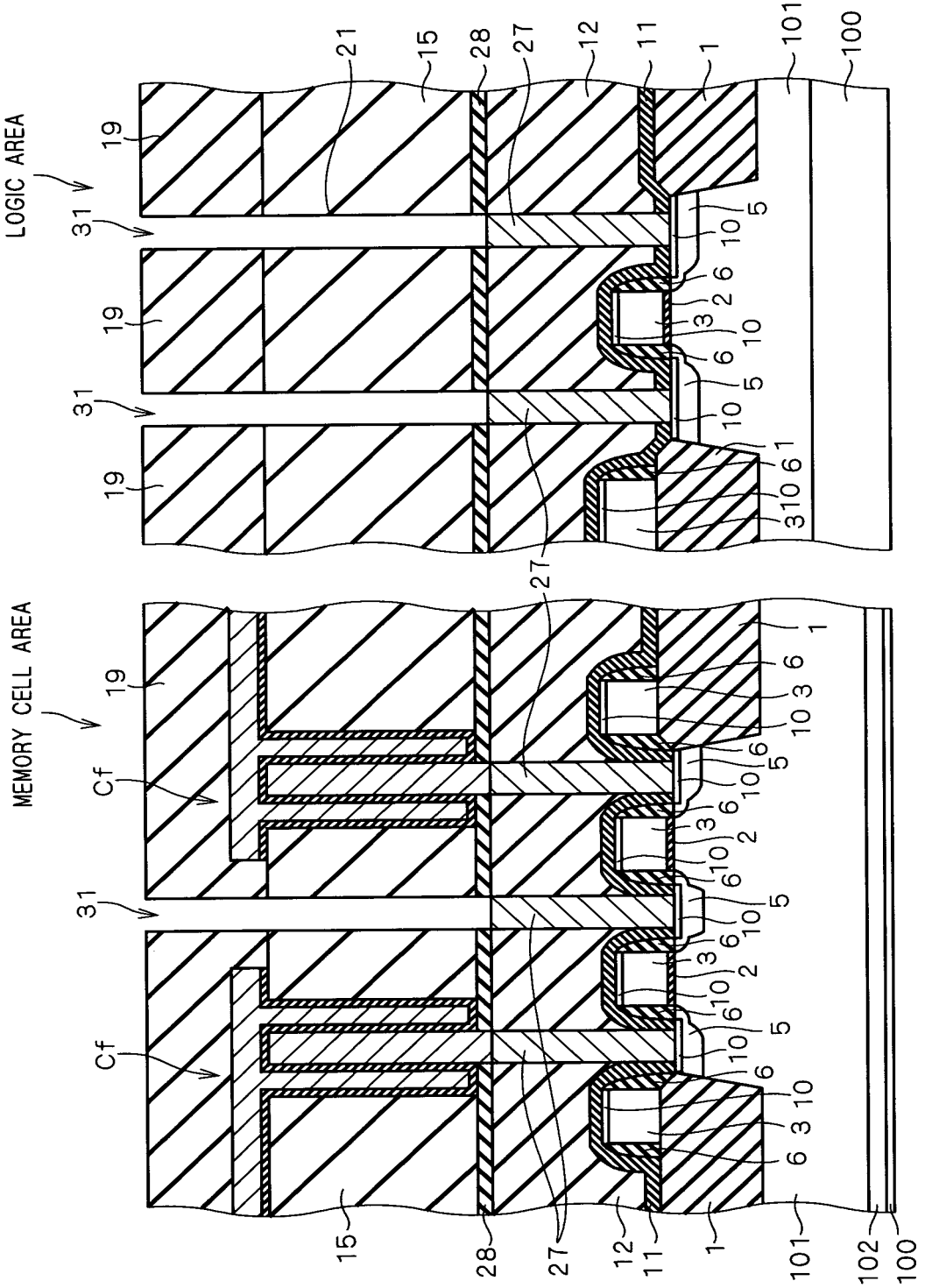

LOGIC AREA
MEMORY CELL AREA
Cf
19
31
21
15
28
27
12
11
1
101
100
102
5
10
6
3
2

FIG. 47

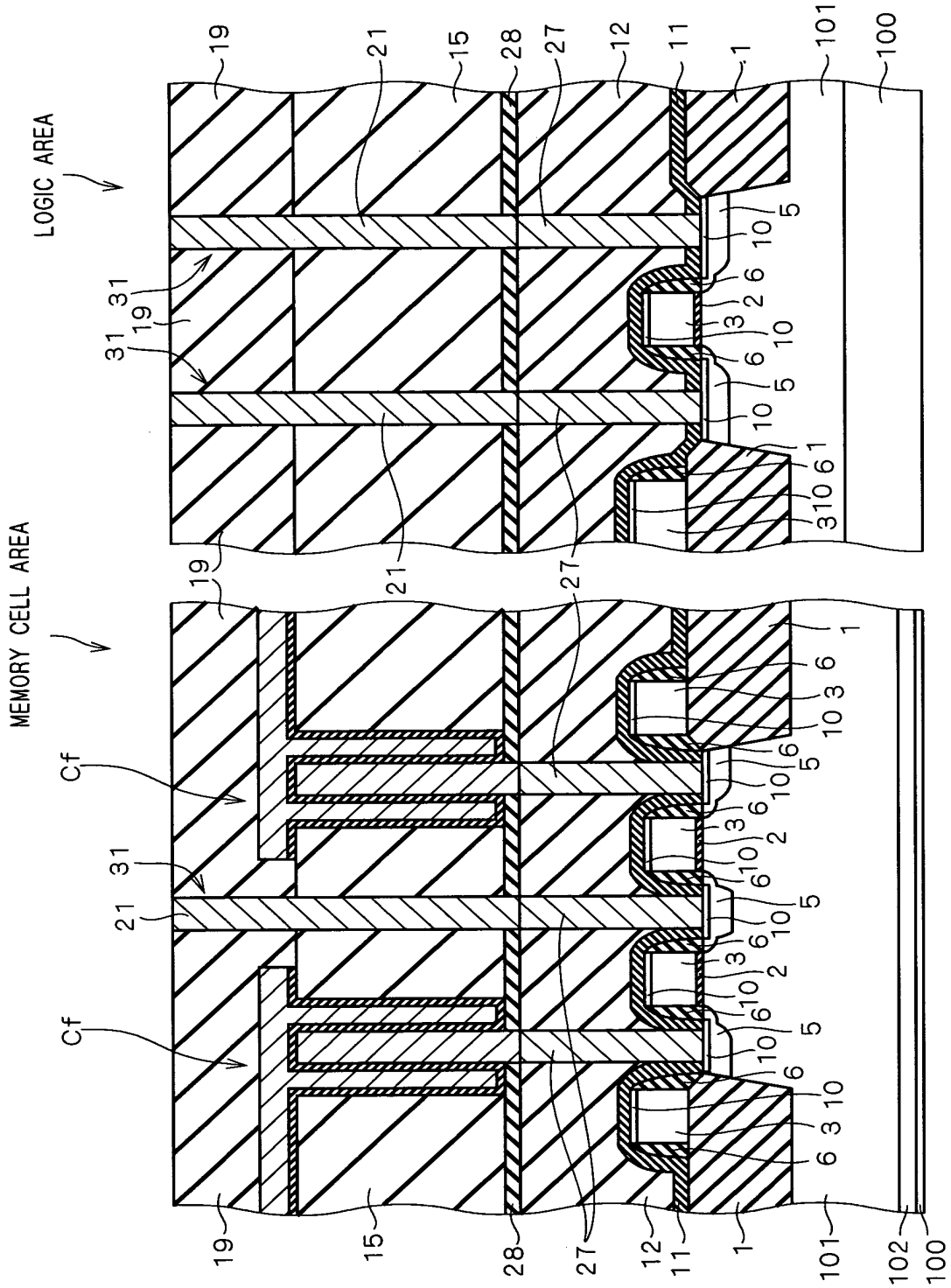

LOGIC AREA
MEMORY CELL AREA
Cf
Cf
19
21
15
28
27
12
11
1
101
100
102
31
5
10
6
2
3

FIG. 48

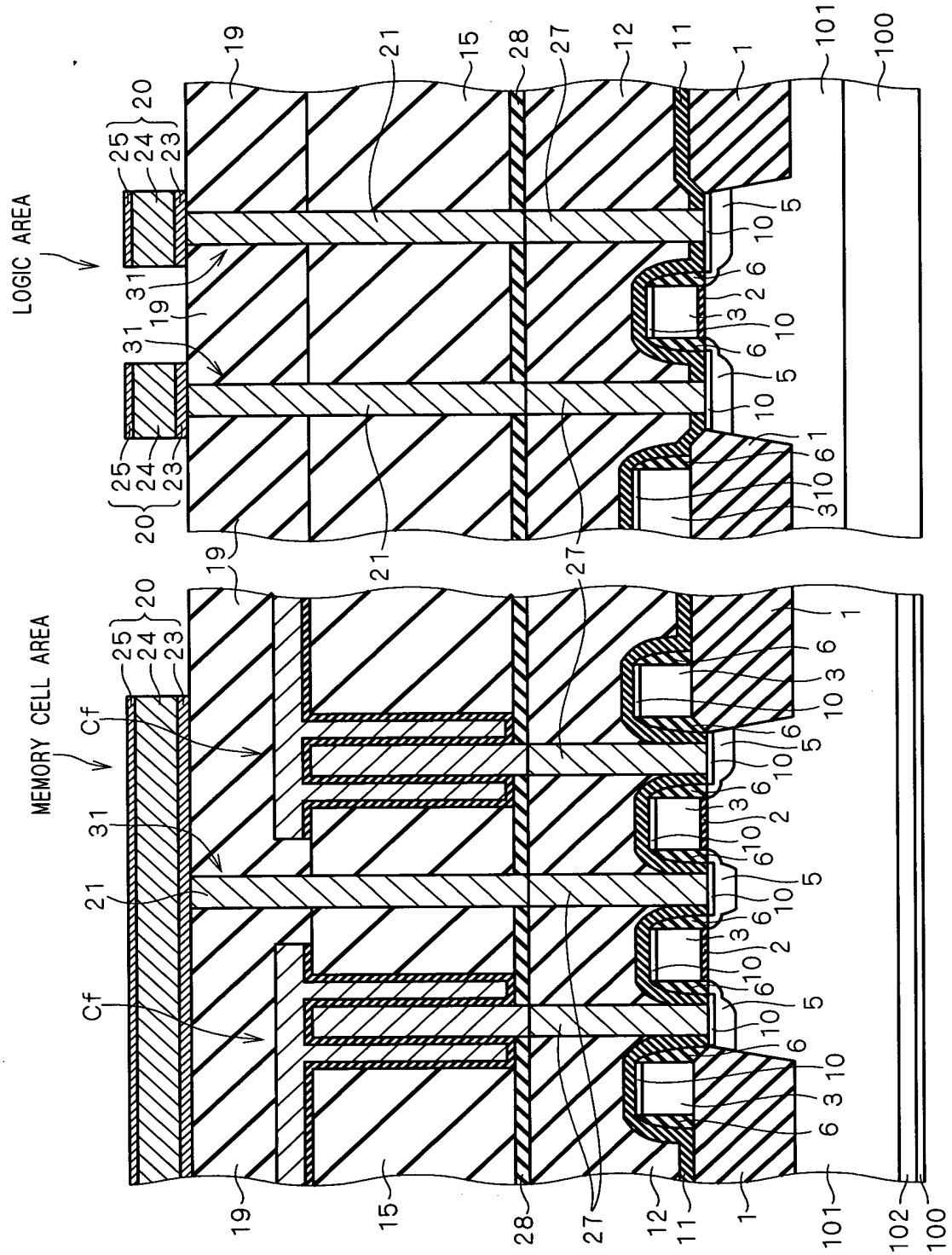

LOGIC AREA
MEMORY CELL AREA
Cf
19
21
15
28
27
12
11
1
101
100
102
20
25
24
23
31
5
10
6
2
3

FIG. 49

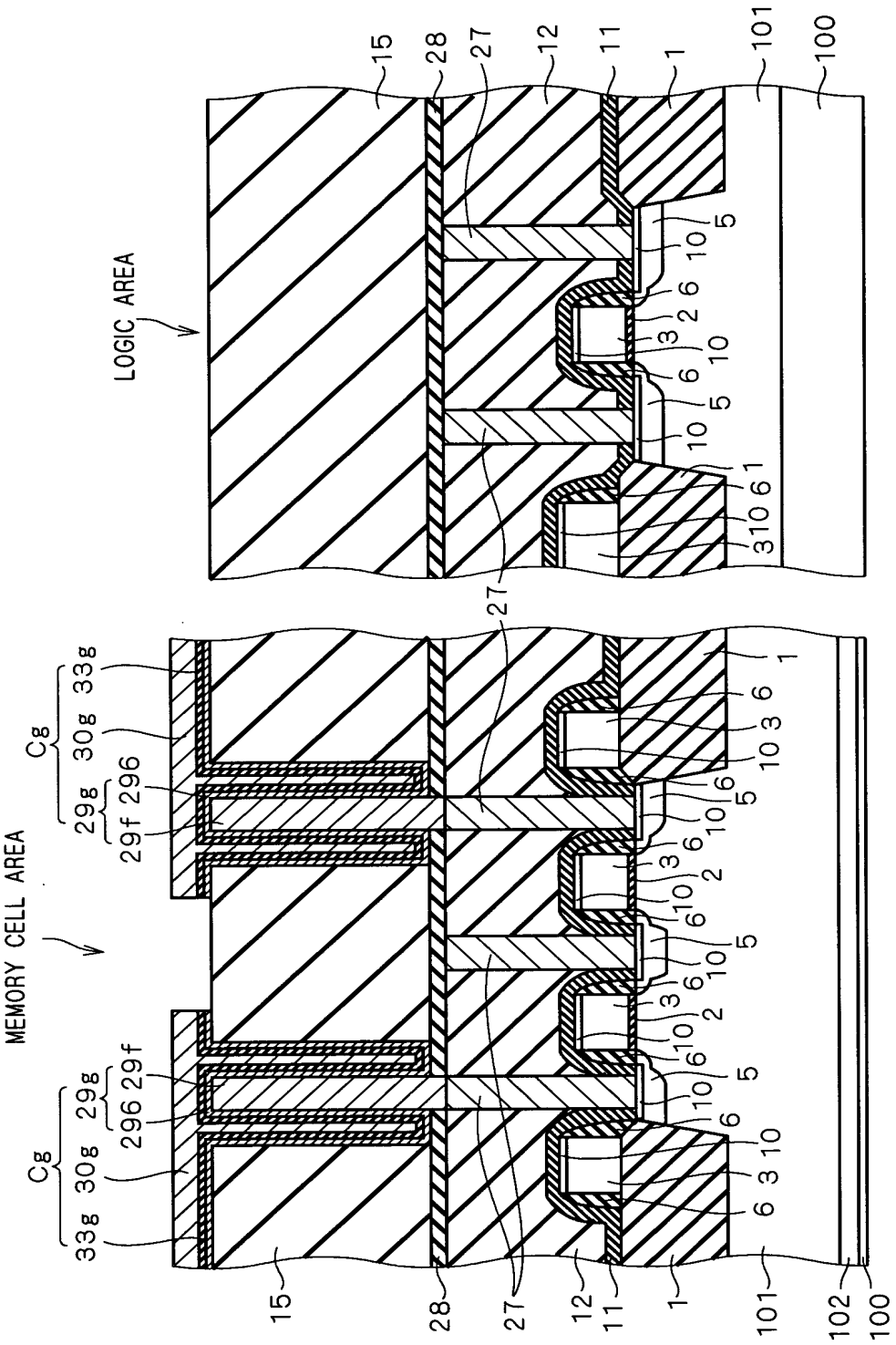
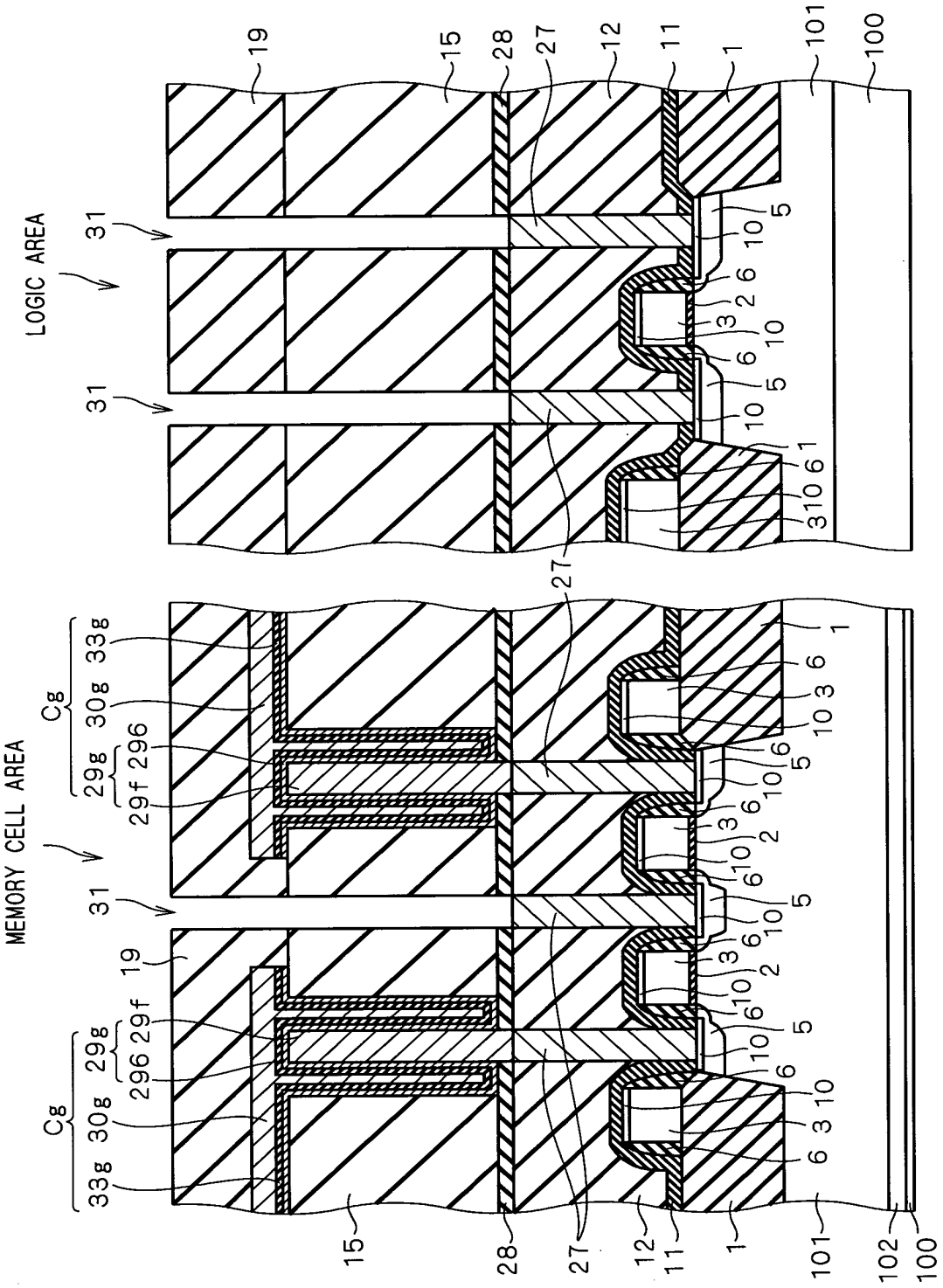

LOGIC AREA
MEMORY CELL AREA
Cg
33g
30g
29g
29f
296
15
28
27
12
11
1
101
102
100
10
5
6
2
3

FIG. 50


LOGIC AREA
MEMORY CELL AREA
31
Cg
33g
30g
29g
29f
296
19
15
28
27
12
11
1
101
102
100
5
10
6
3
2

F I G . 5 1

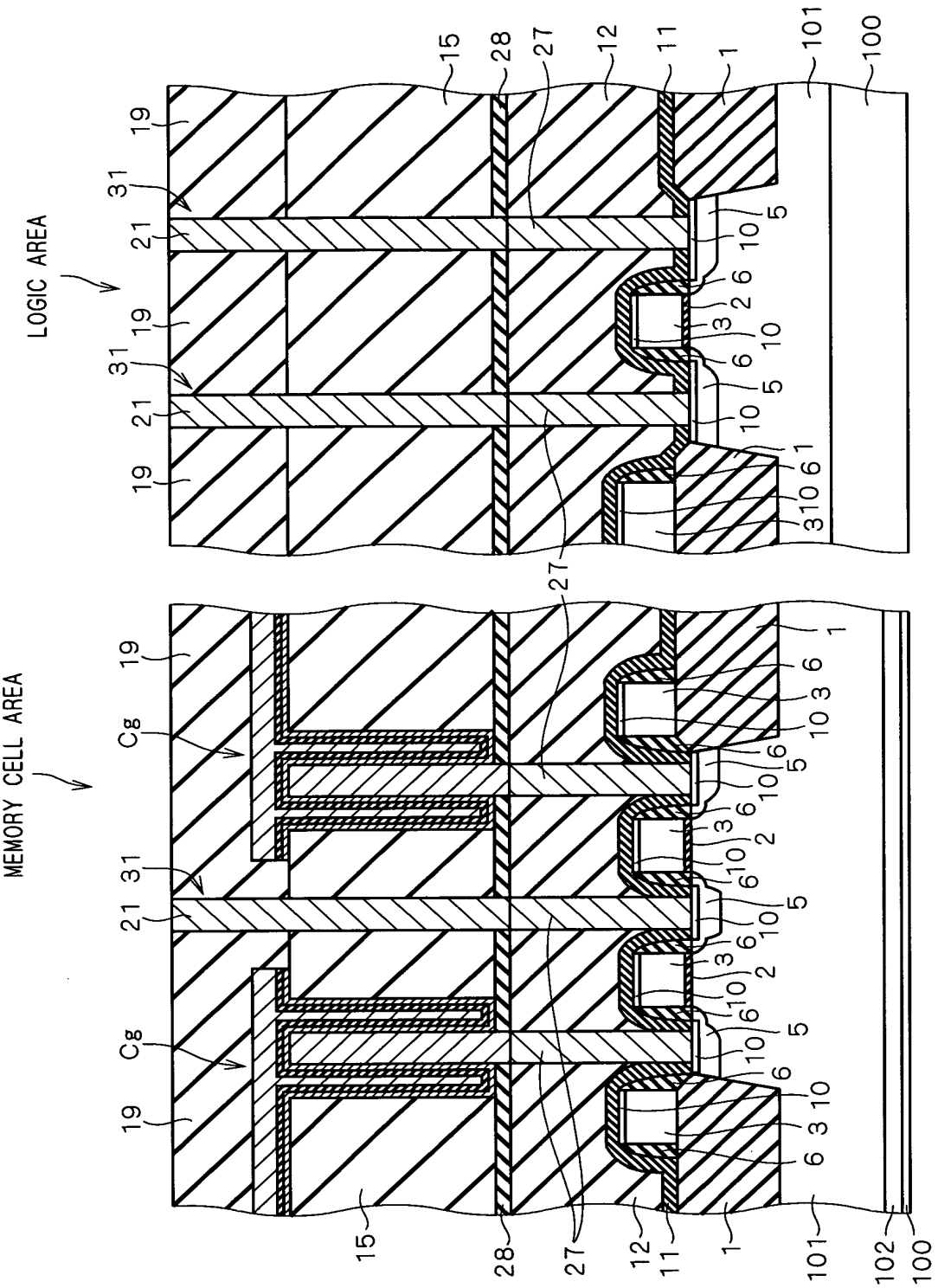


FIG. 52

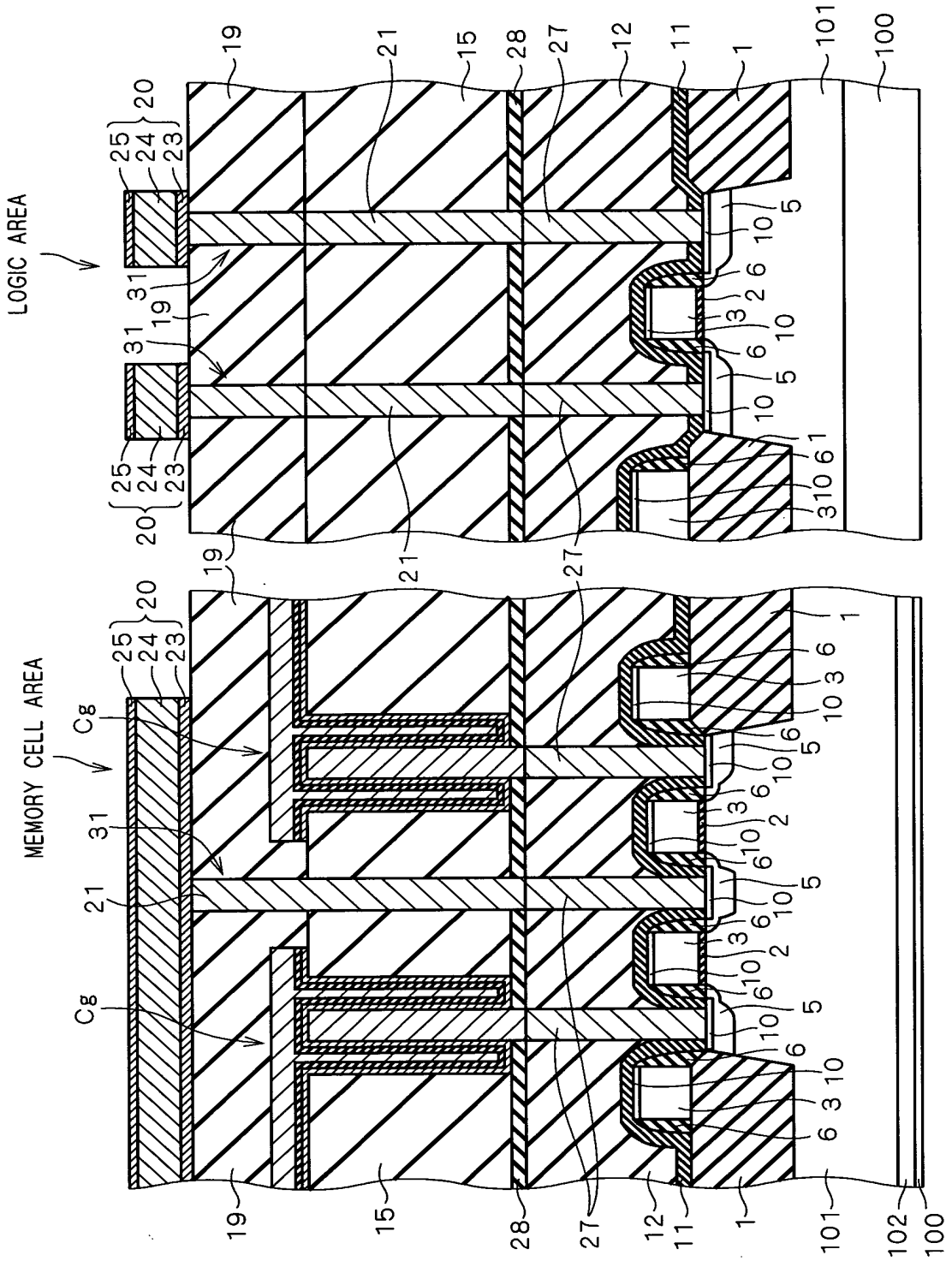

LOGIC AREA
MEMORY CELL AREA
Cg
19
21
15
28
27
12
11
1
101
102
100
20
25
24
23
31
5
10
6
3
2

FIG. 53

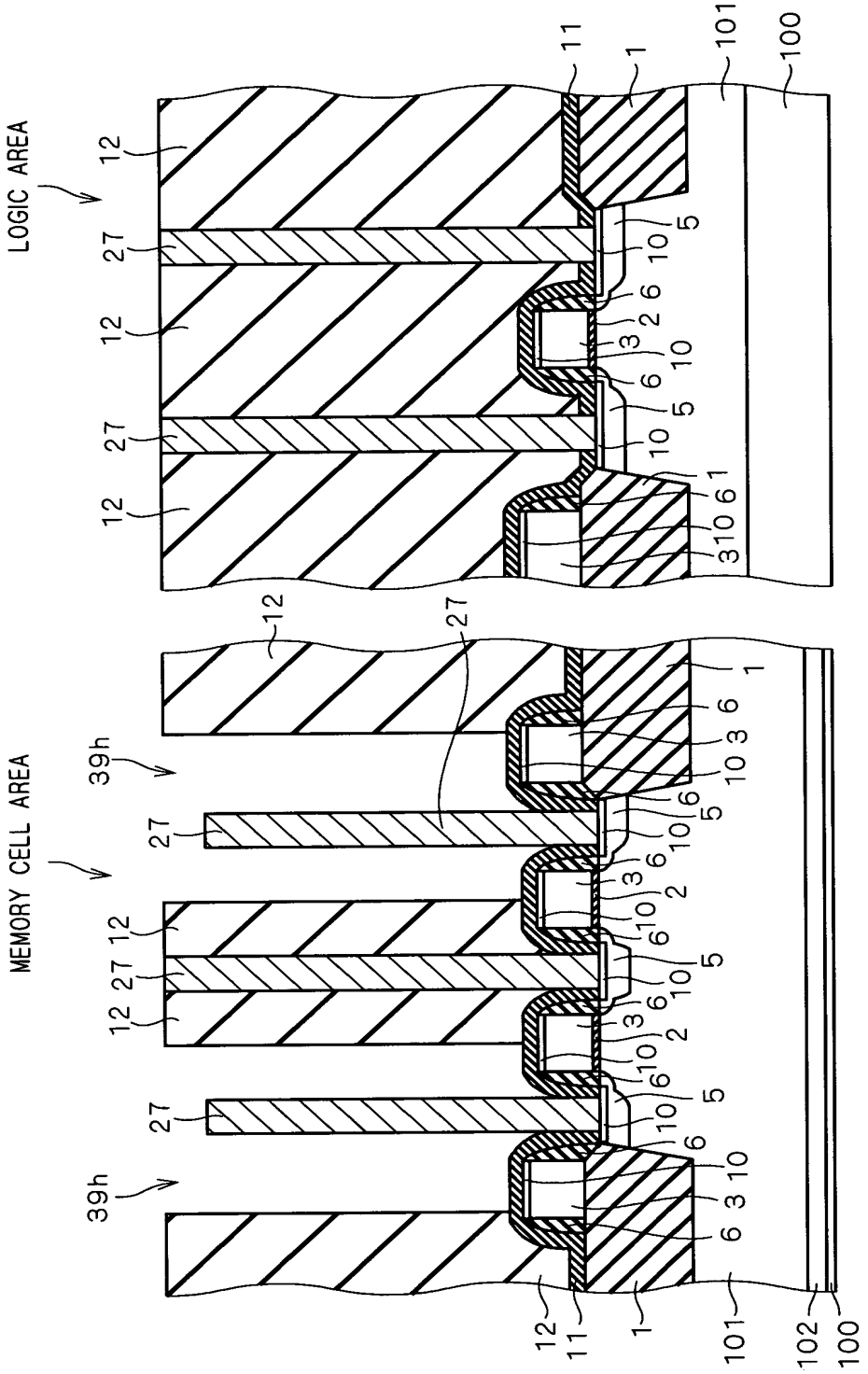


FIG. 54

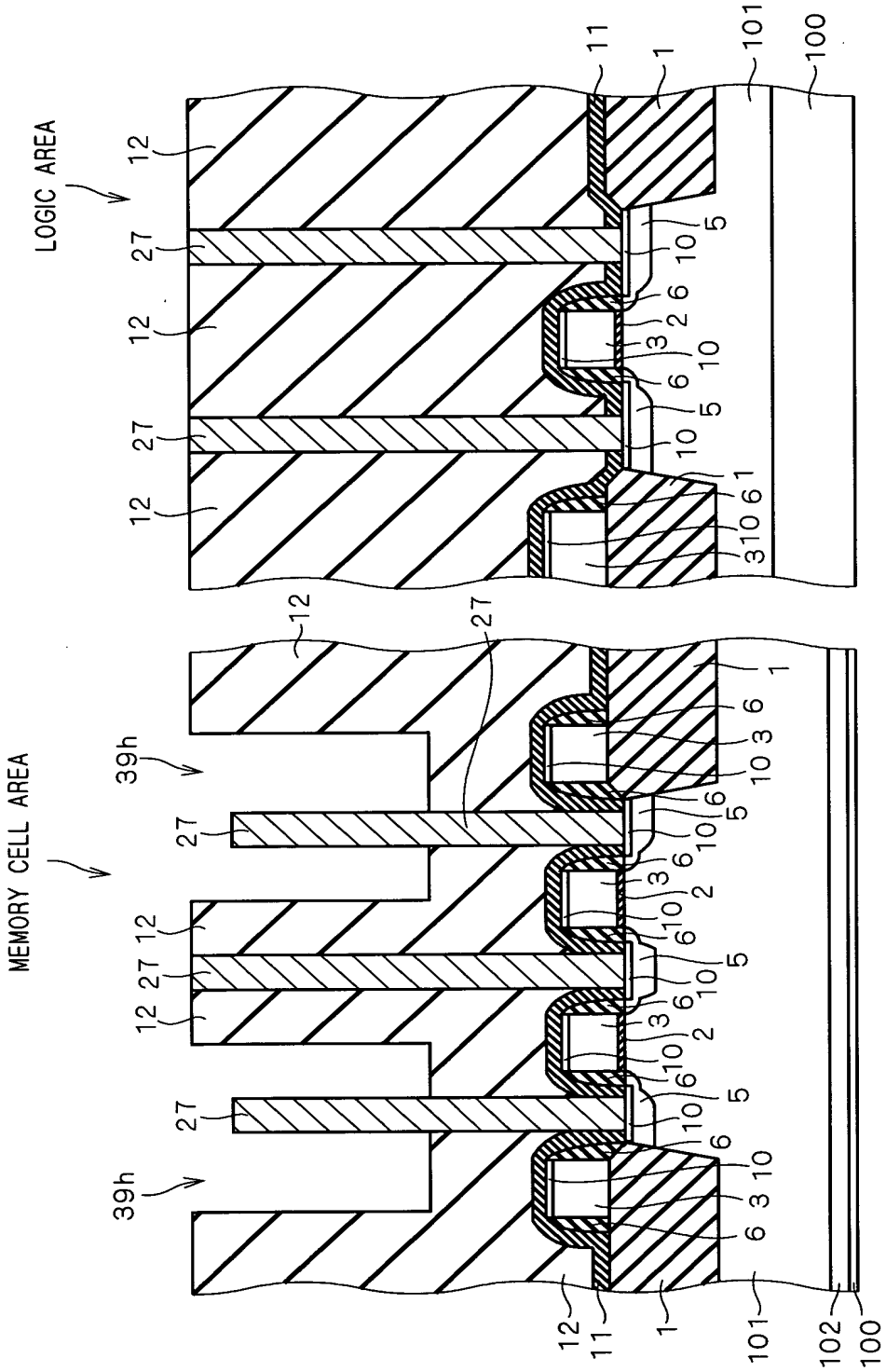

LOGIC AREA
MEMORY CELL AREA
39h
39h
12
27
11
1
101
100
102
5
10
6
3
2

FIG. 55

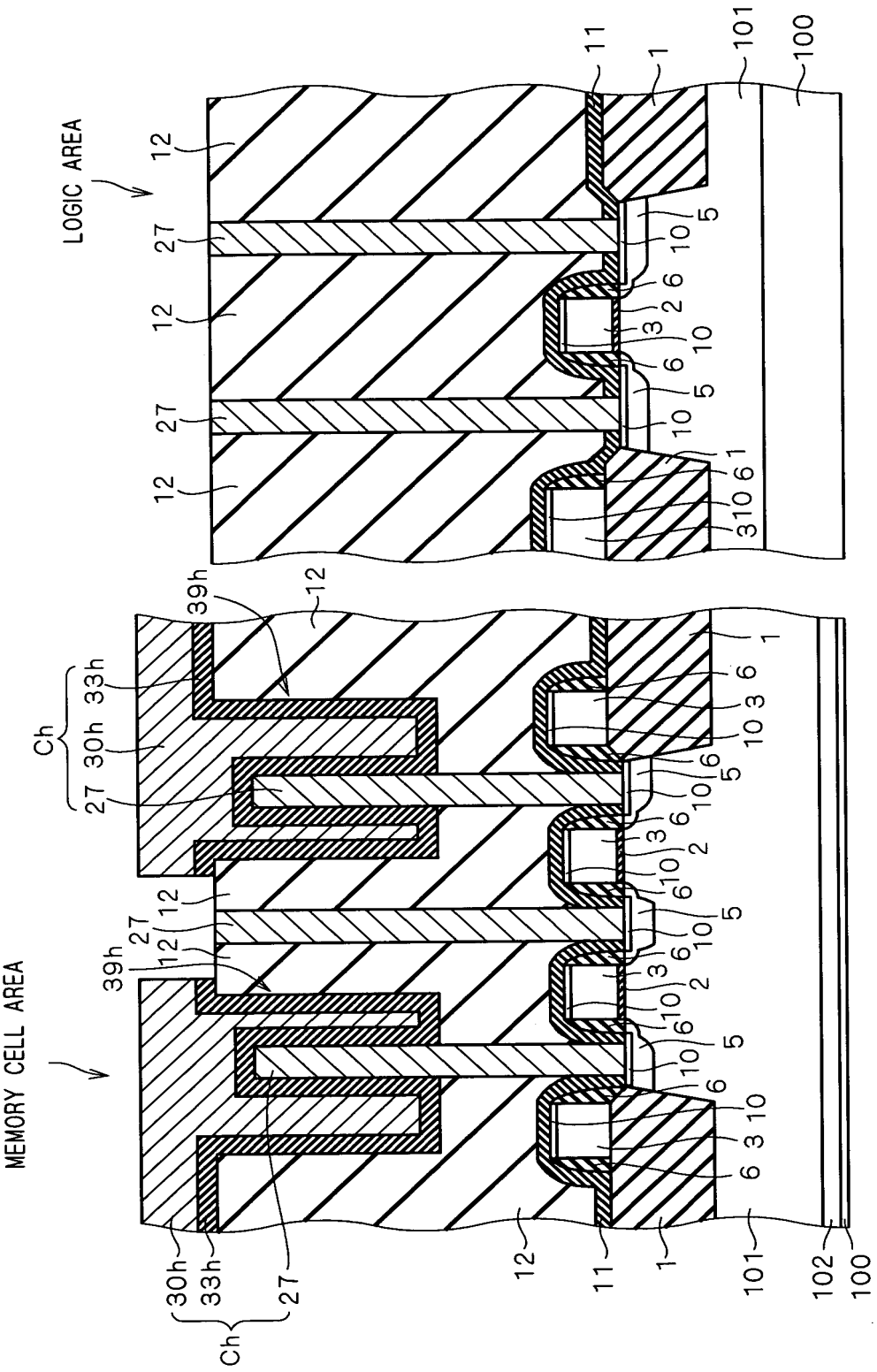

LOGIC AREA
MEMORY CELL AREA
Ch
30h
33h
27
39h
12
11
1
101
100
102
10
6
5
3
2

FIG. 56

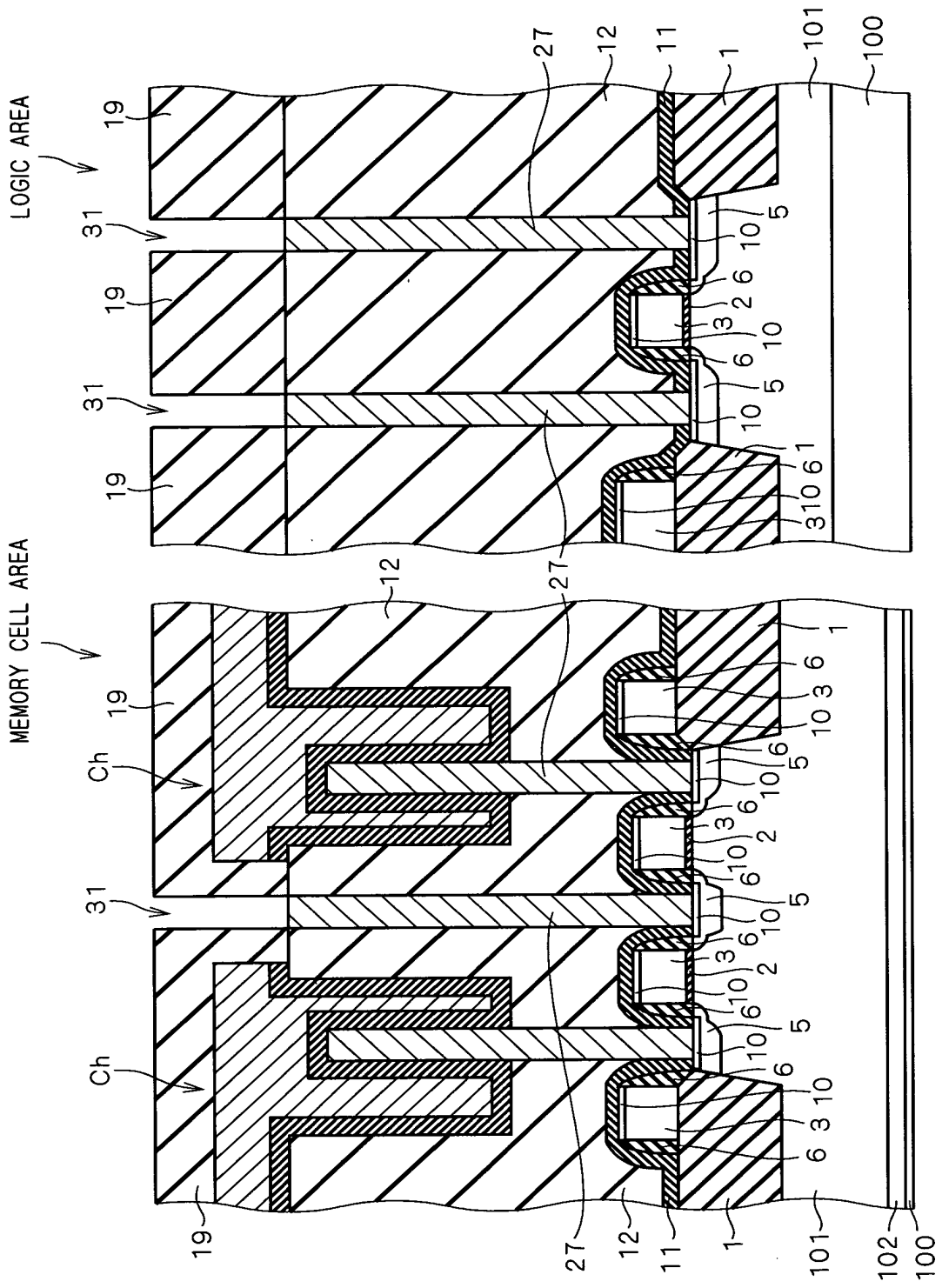

LOGIC AREA
MEMORY CELL AREA
Ch
Ch
19
31
27
12
11
1
101
102
100
5
10
6
3
2

FIG. 57

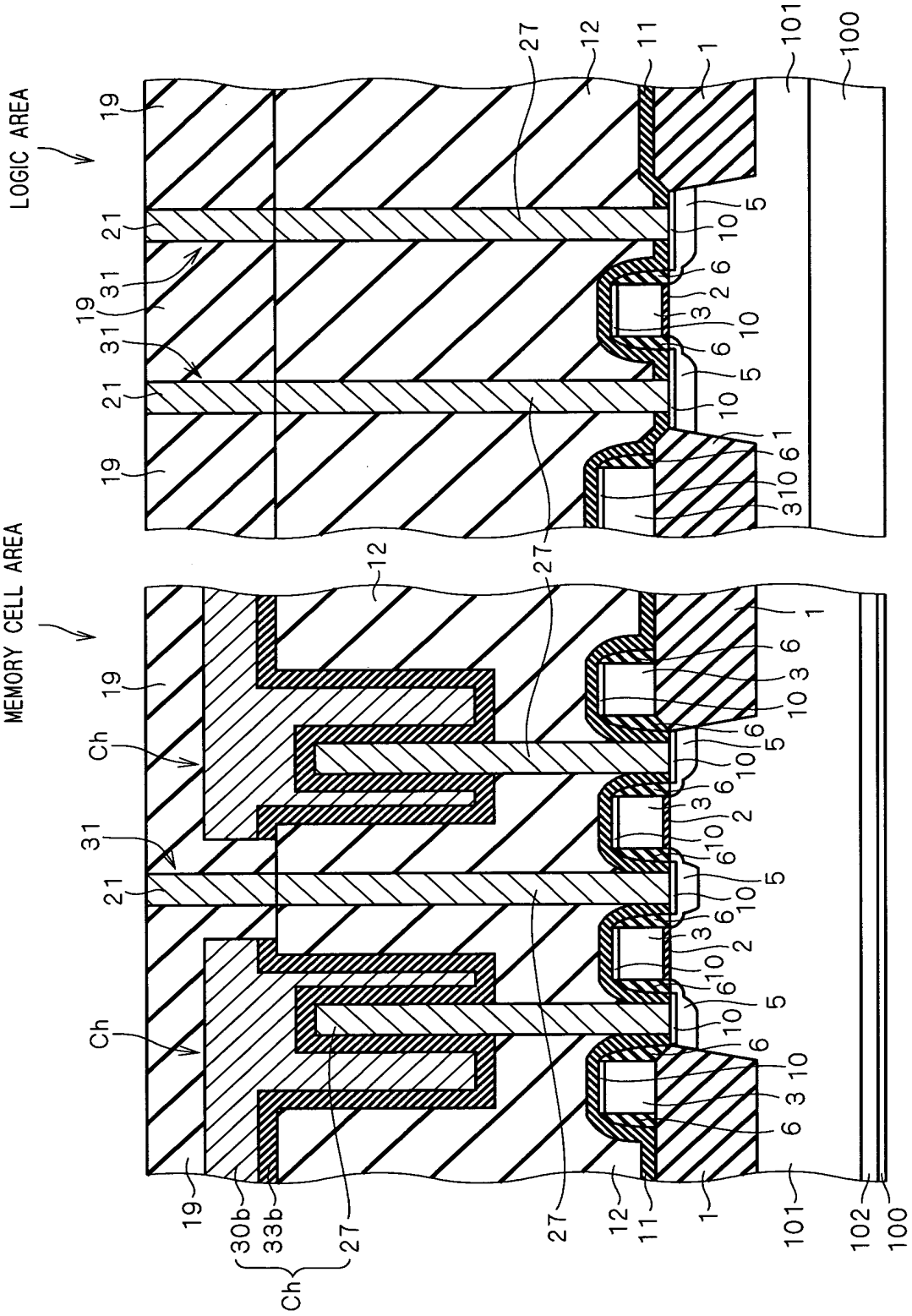

LOGIC AREA
MEMORY CELL AREA
19
21
31
Ch
30b
33b
27
12
11
1
101
102
100
5
10
6
3
2

FIG. 58

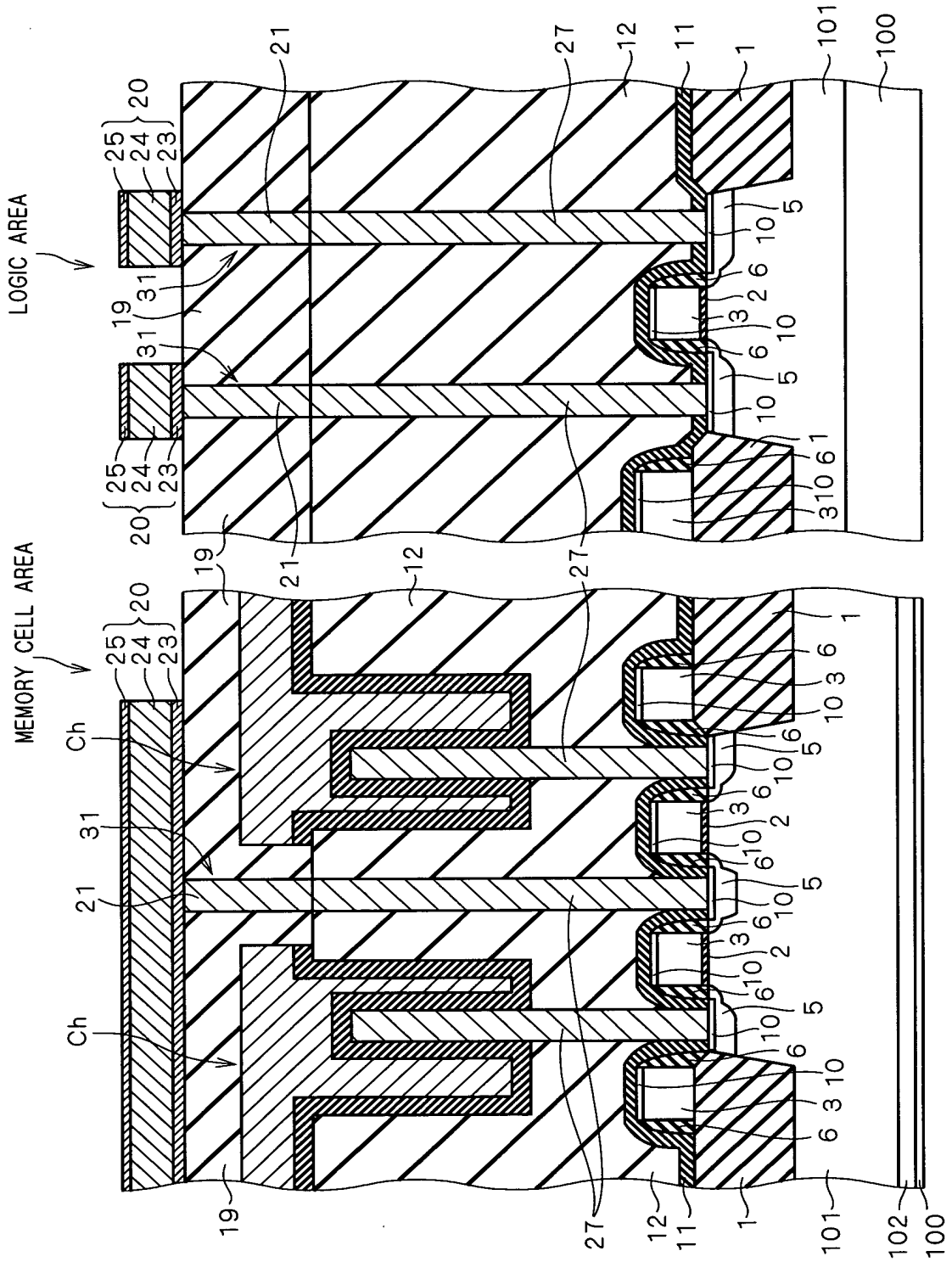

LOGIC AREA
MEMORY CELL AREA
Ch
Ch
19
20
21
23
24
25
27
31
1
2
3
5
6
10
11
12
100
101
102

FIG. 59

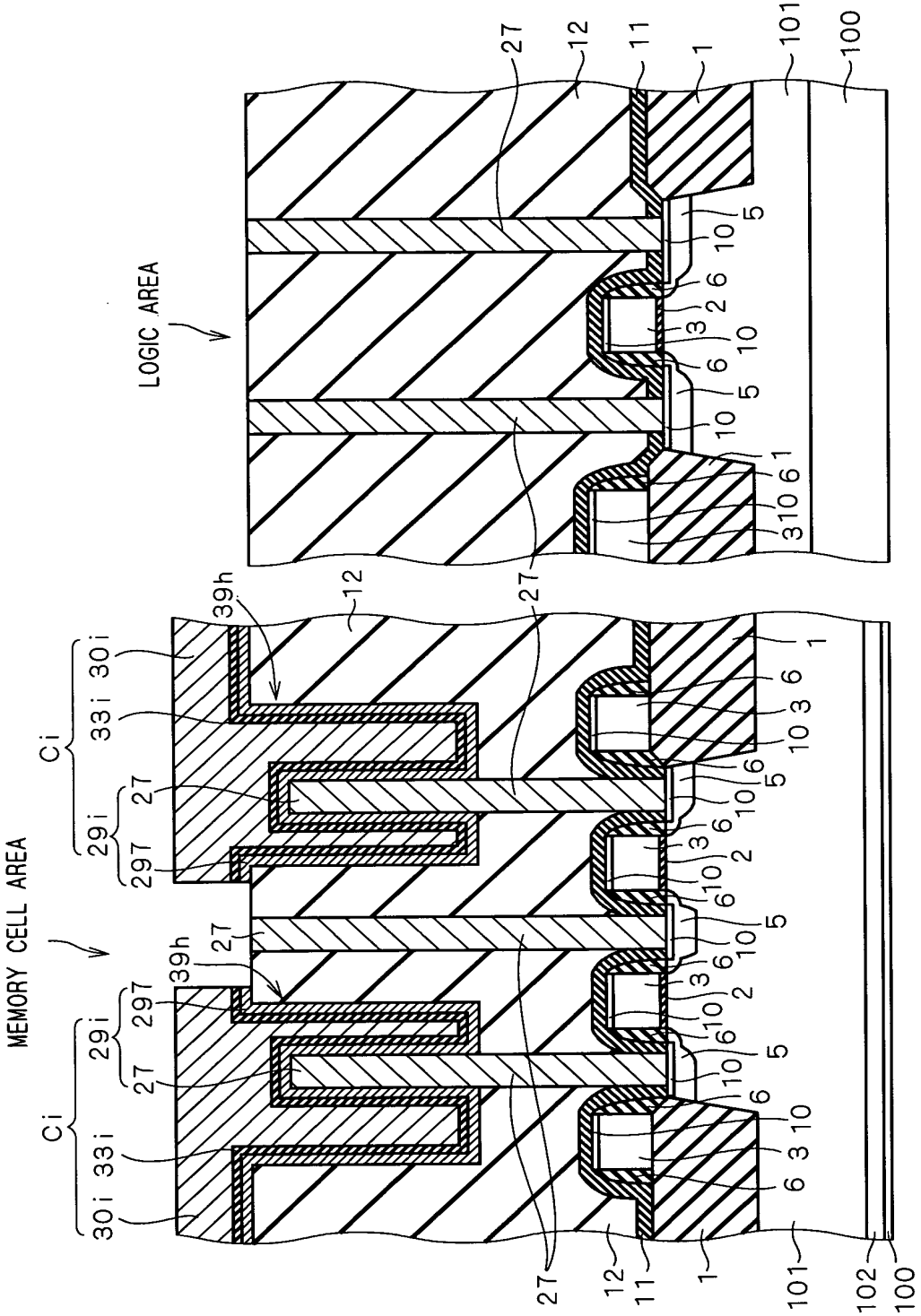

LOGIC AREA
MEMORY CELL AREA
Ci
30i
33i
29i
297
27
39h
12
11
1
101
100
102
10
6
5
3
2

FIG. 60

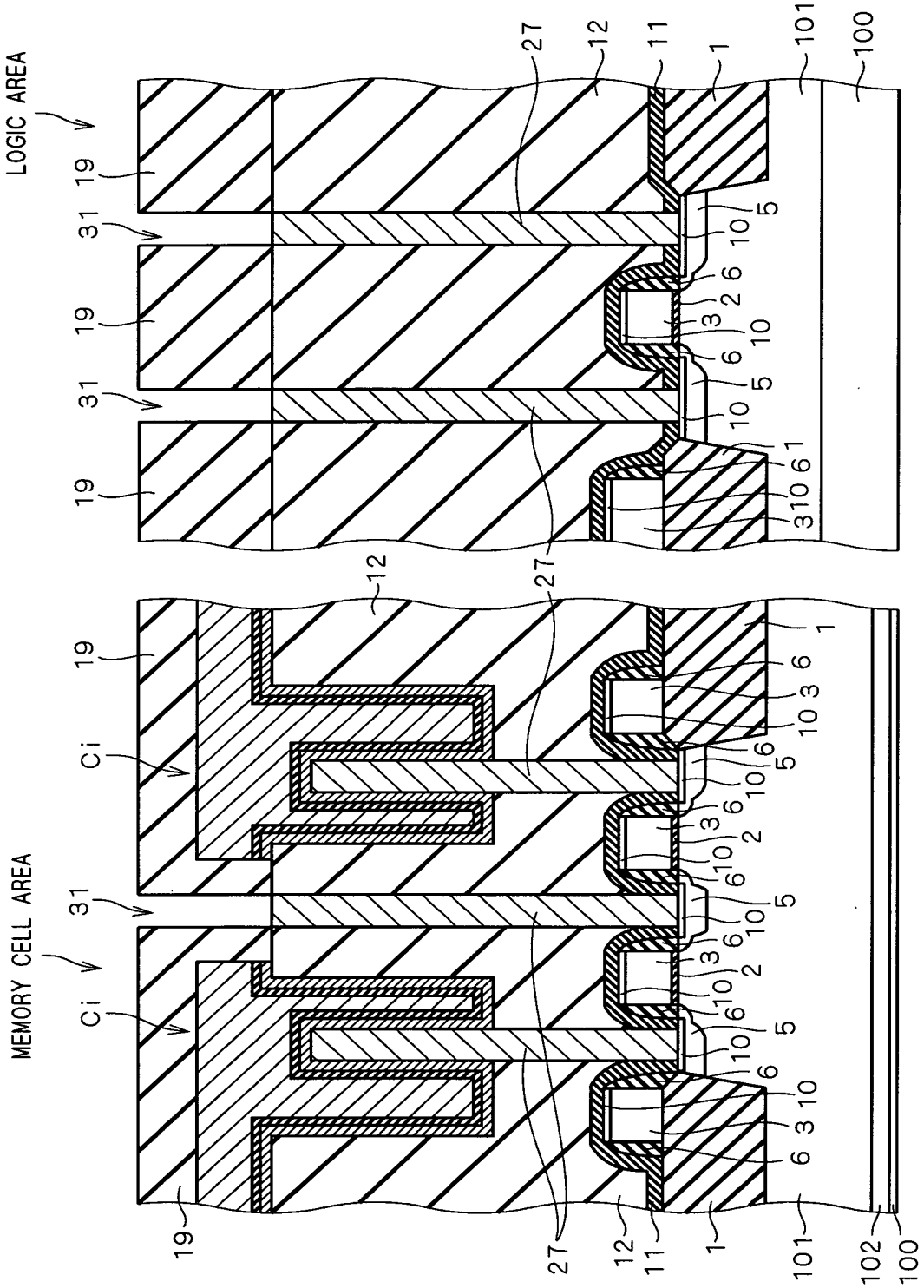

LOGIC AREA
MEMORY CELL AREA
19
31
Ci
27
12
11
1
101
100
102
5
10
6
2
3

FIG. 61

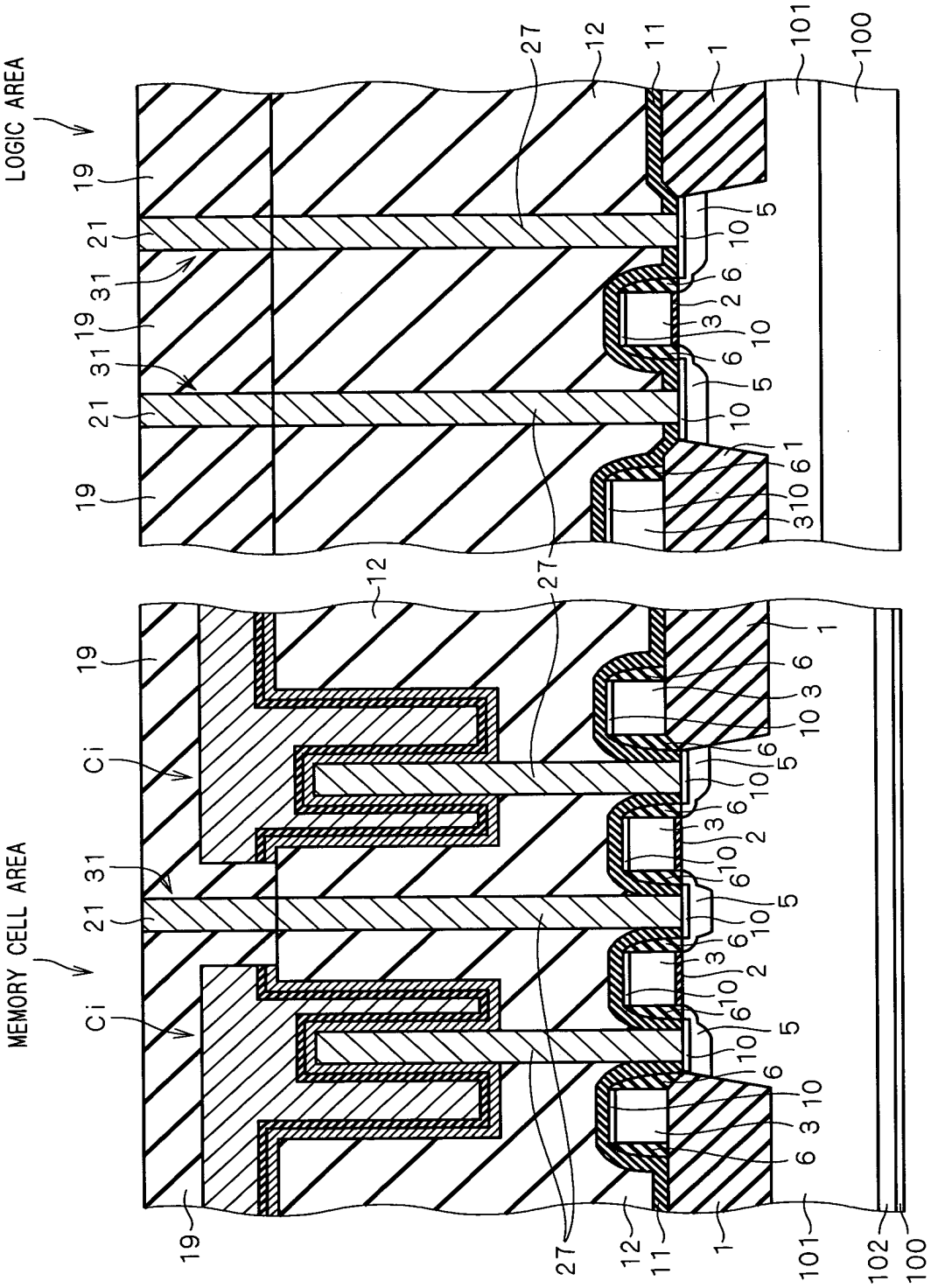

LOGIC AREA
MEMORY CELL AREA
Ci
19
21
31
27
12
11
1
101
100
102
5
10
6
2
3

FIG. 62

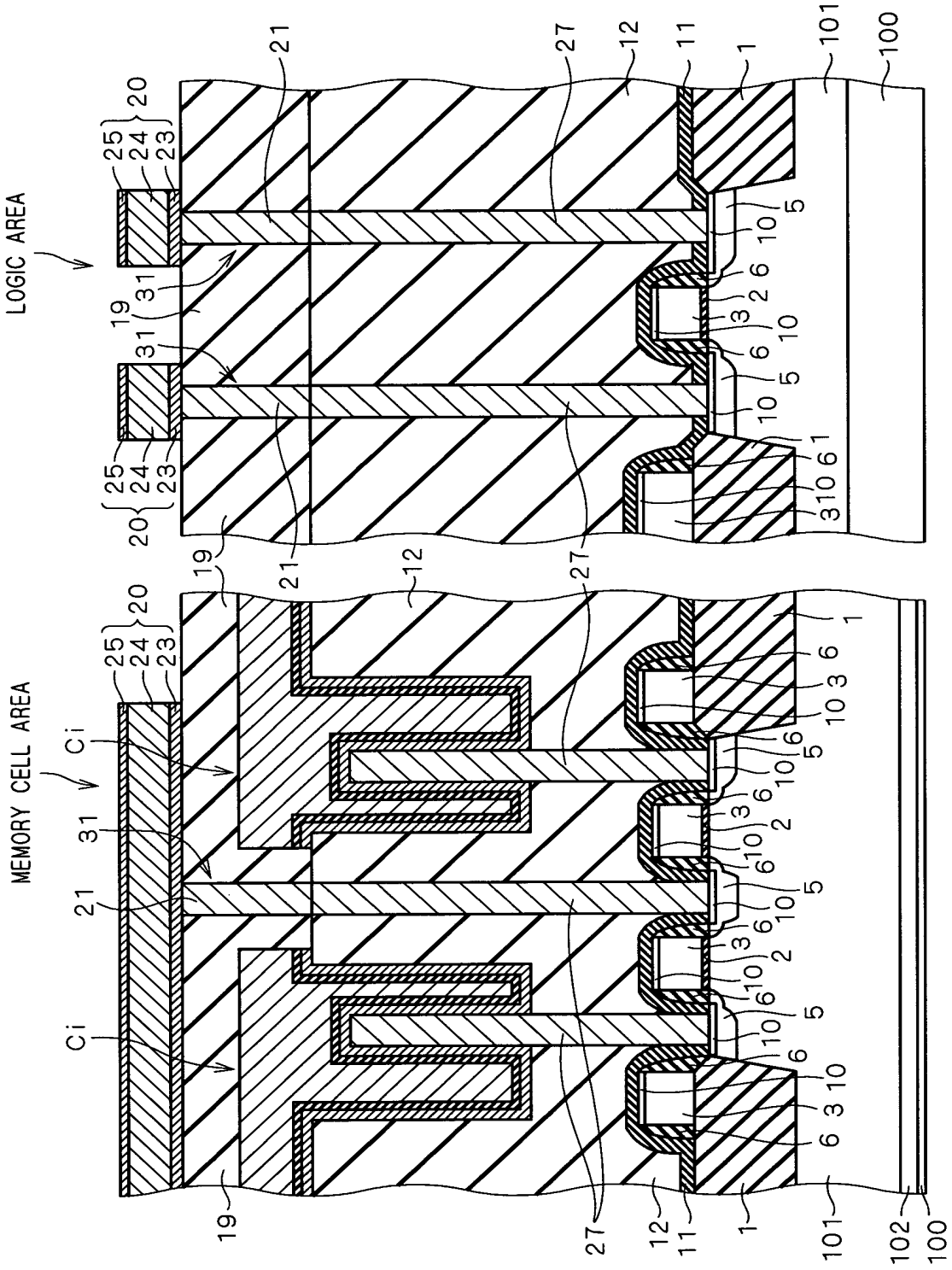

LOGIC AREA
MEMORY CELL AREA
Ci
Ci
19
20
21
23
24
25
27
31
1
2
3
5
6
10
11
12
100
101
102

FIG. 63

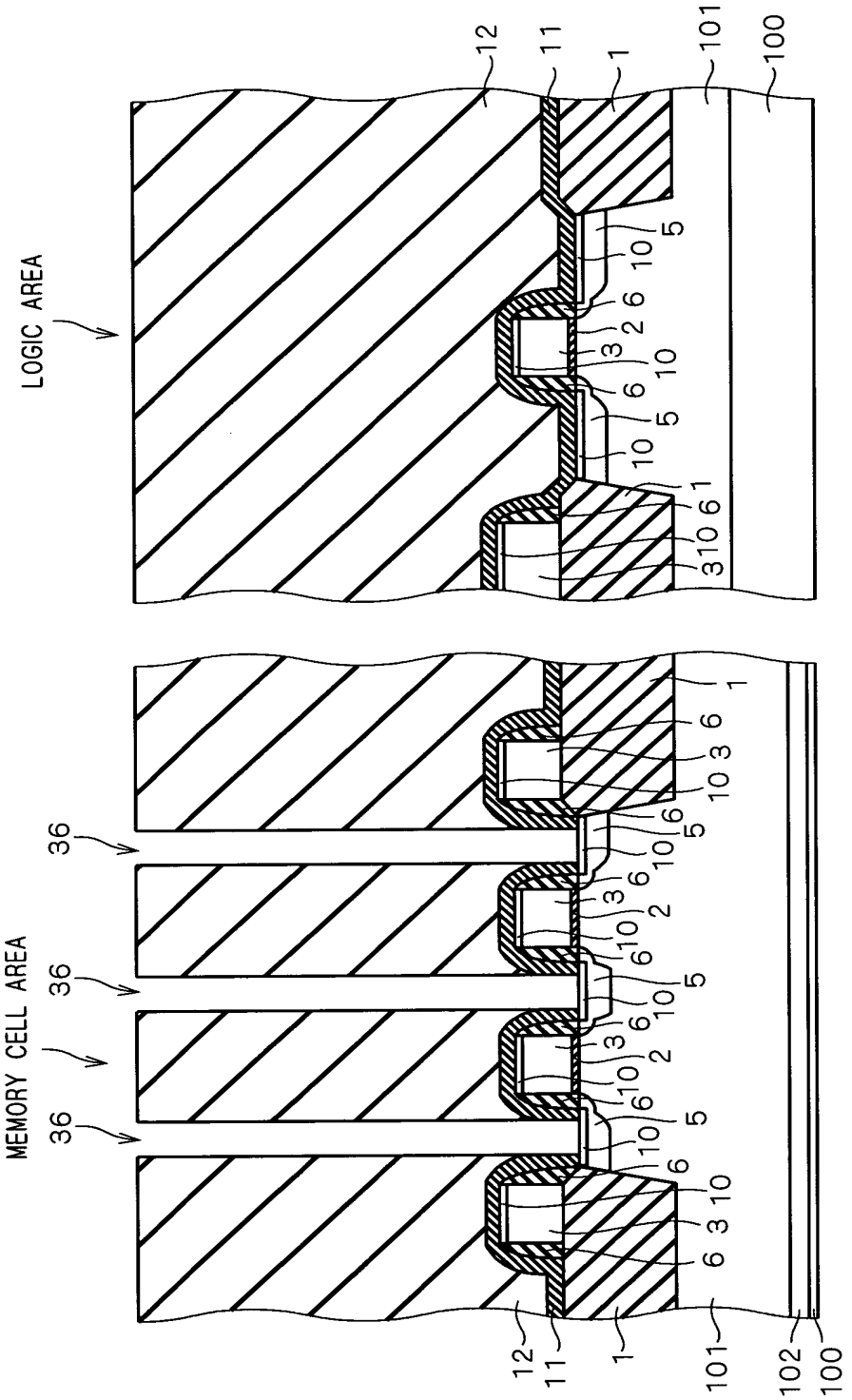


FIG. 64

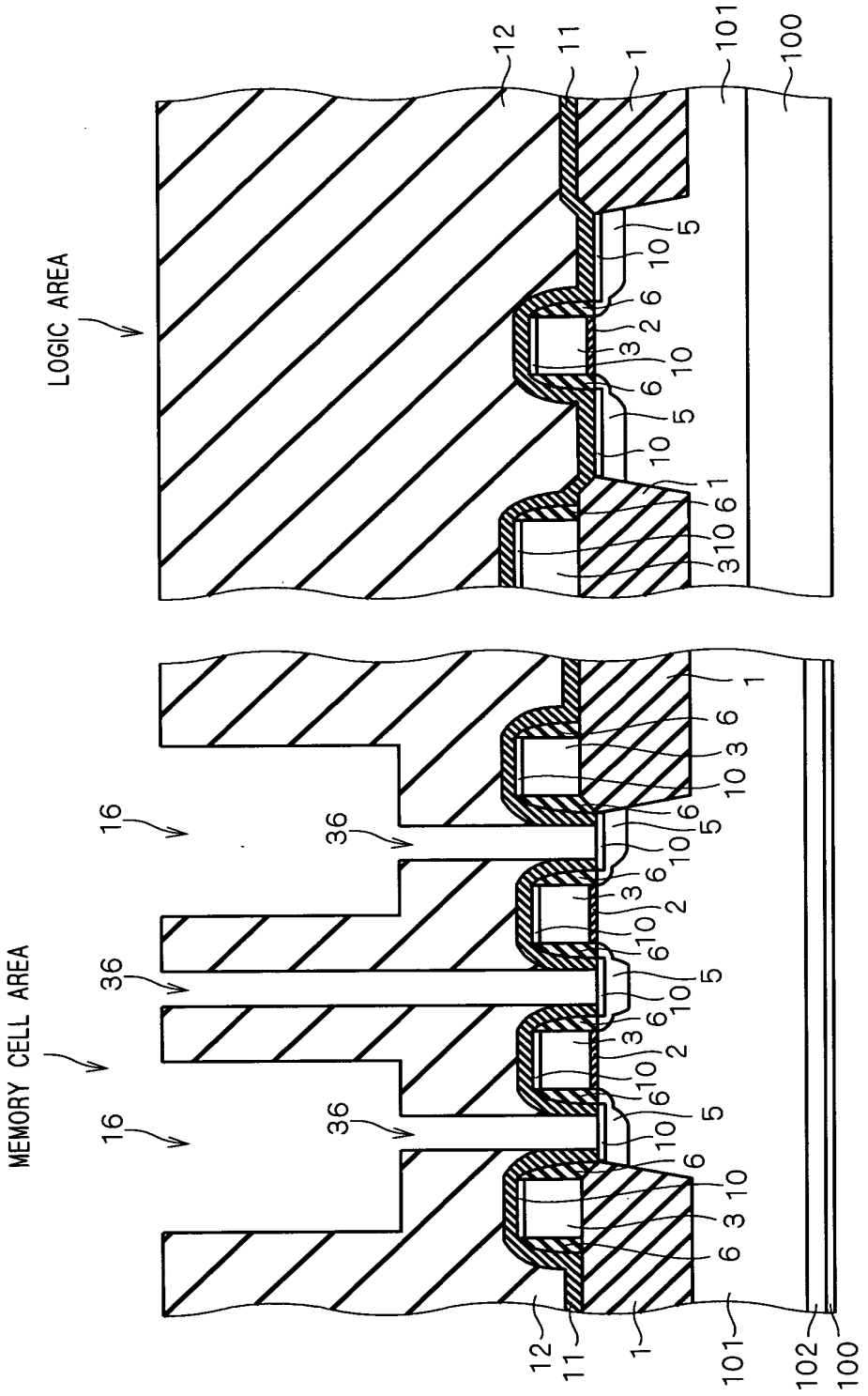


FIG. 65

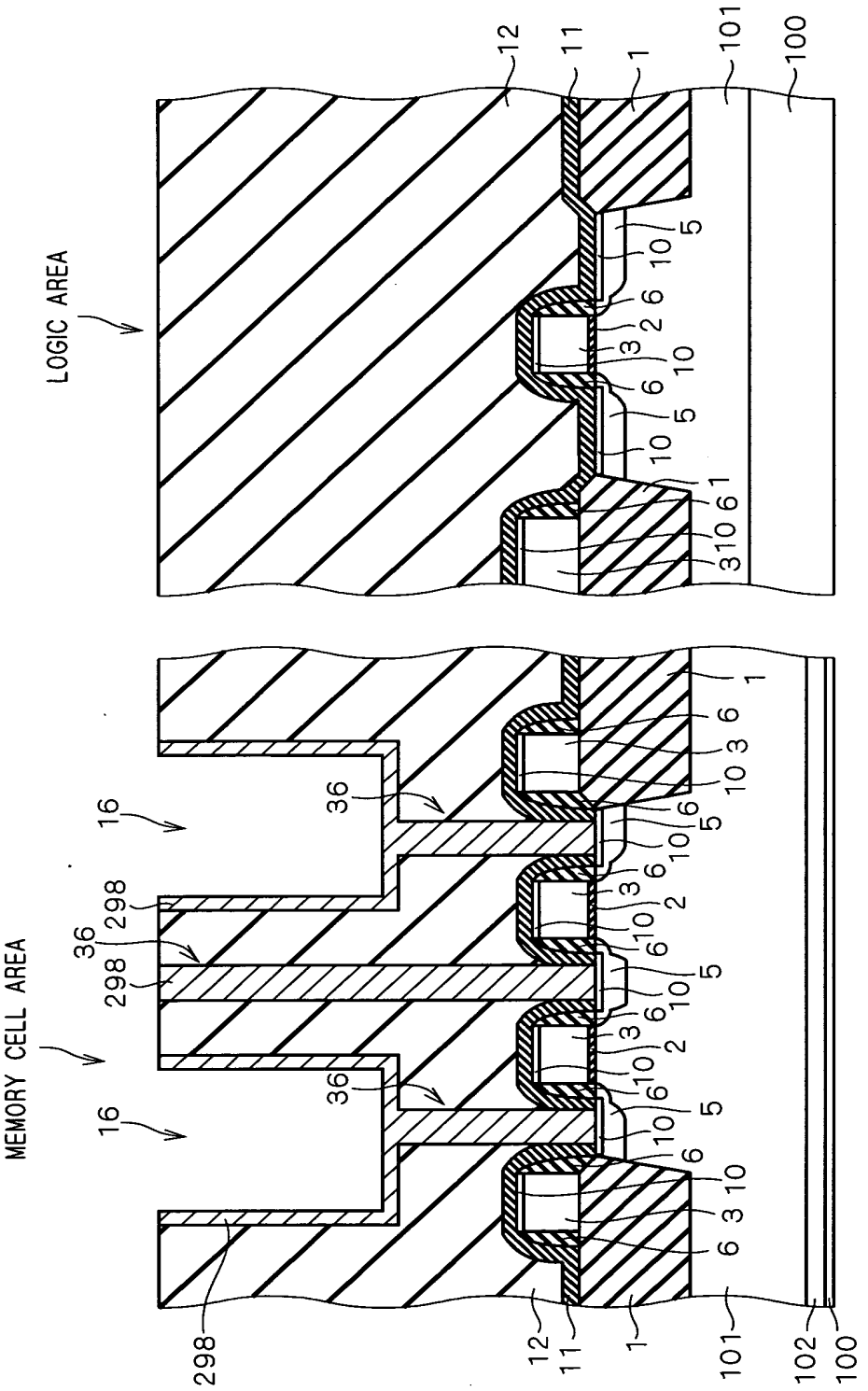

LOGIC AREA
MEMORY CELL AREA
12
11
1
101
100
102
16
36
298
5
10
6
2
3

FIG. 66

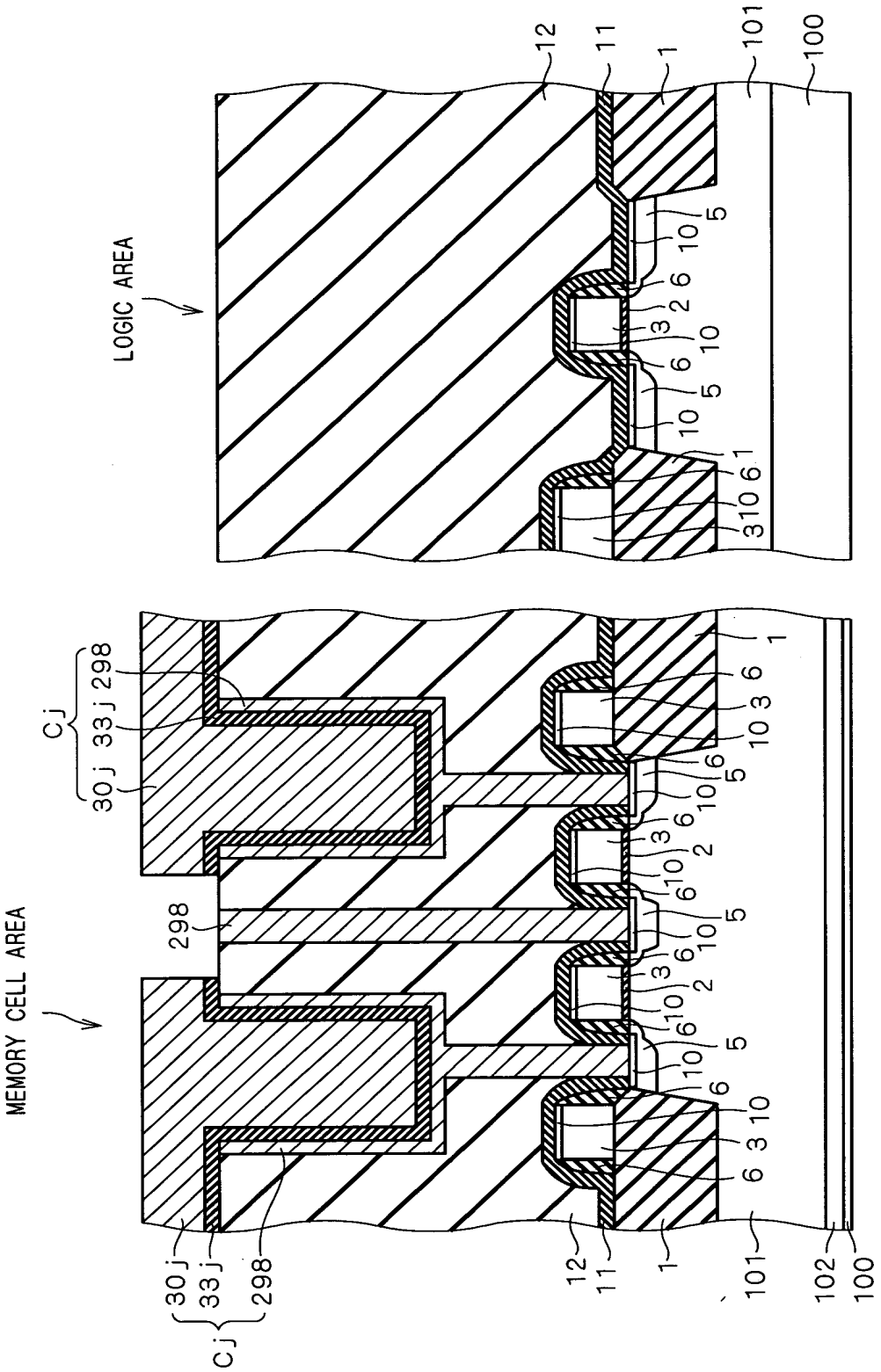


FIG. 67

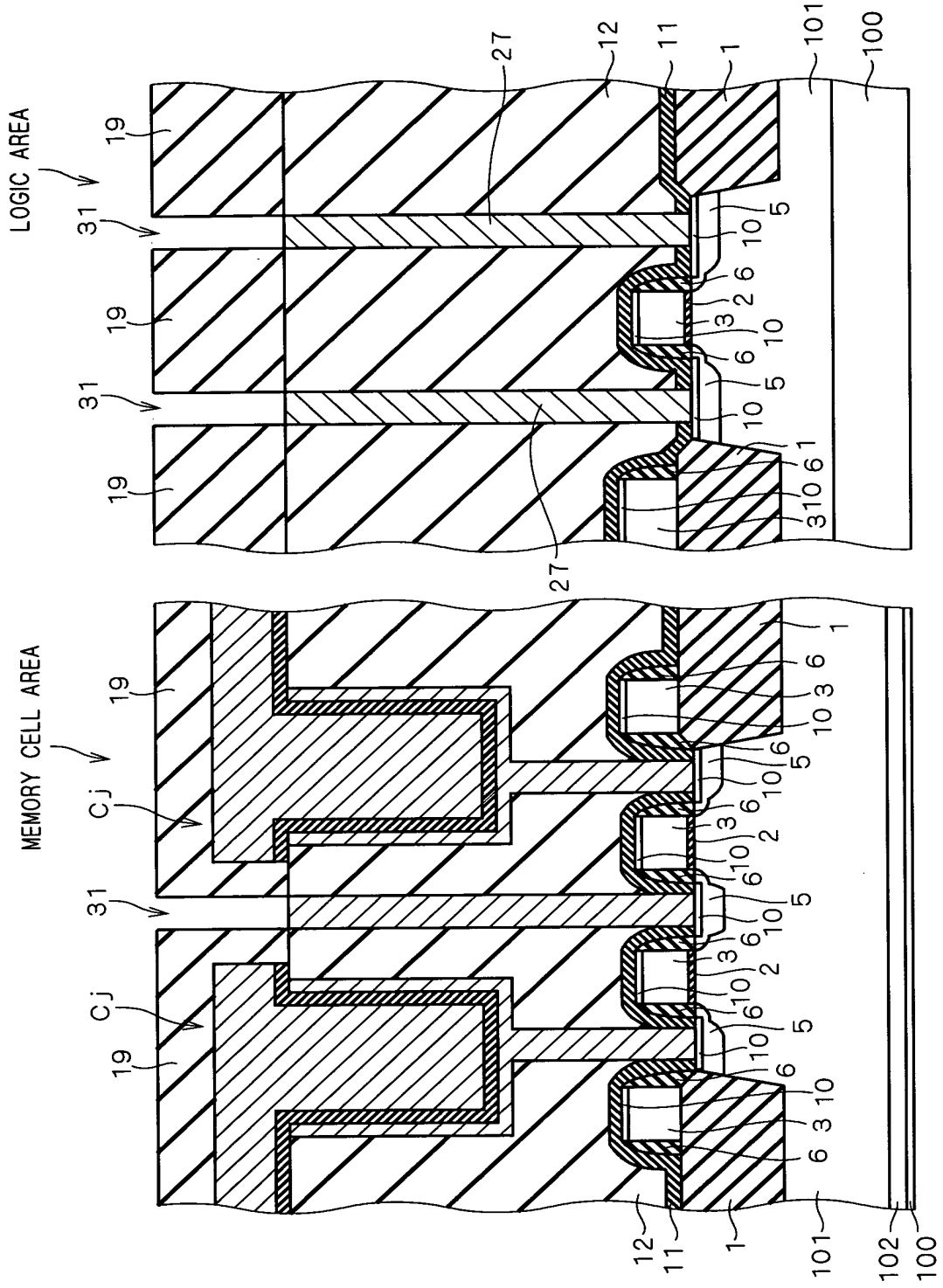

LOGIC AREA
MEMORY CELL AREA
Cj
19
31
27
12
11
1
101
100
102
5
10
6
2
3

FIG. 68

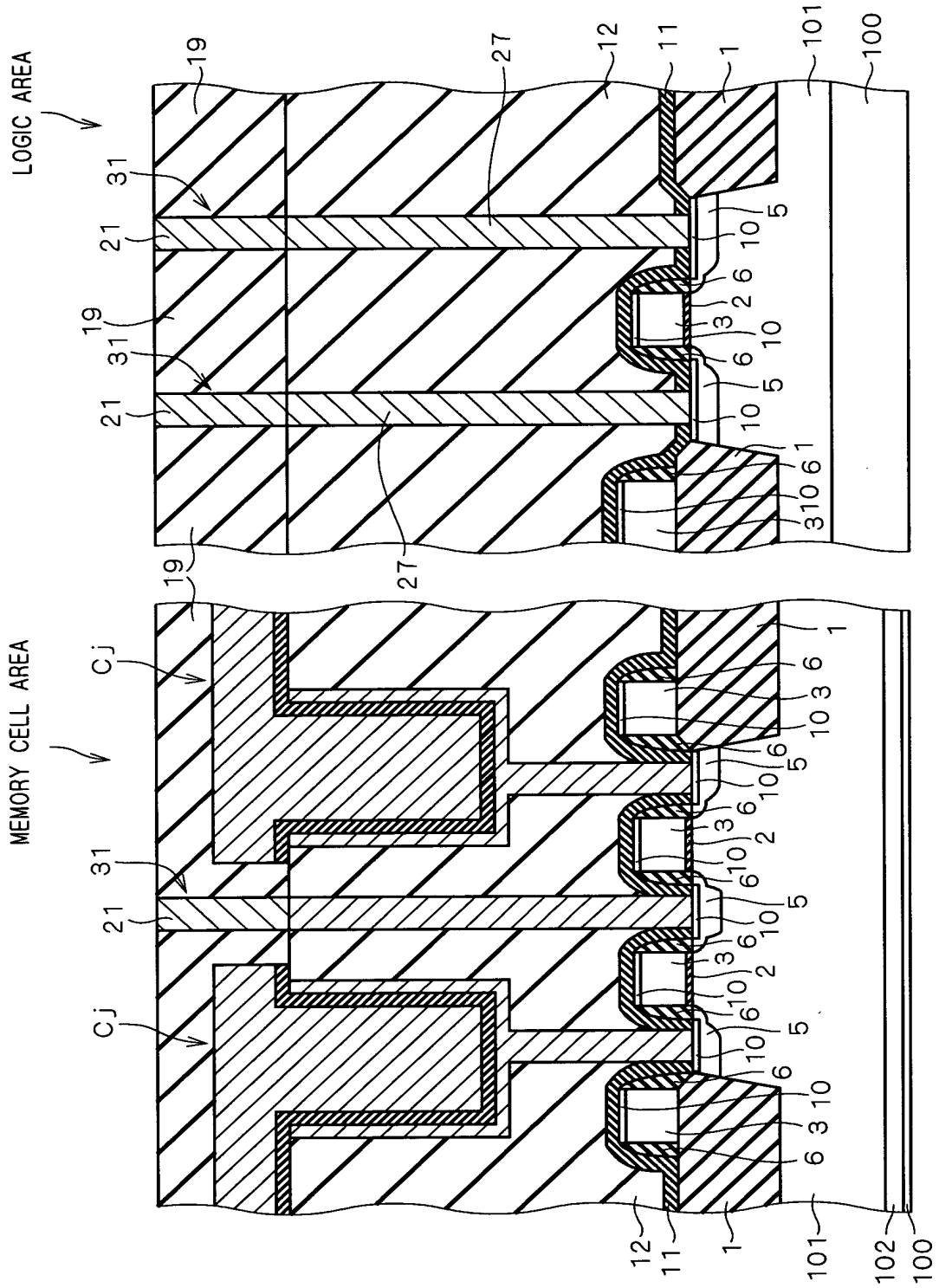

LOGIC AREA
MEMORY CELL AREA
19
27
12
11
1
101
100
31
21
Cj
10
5
6
3
2
61
310
102

FIG. 69

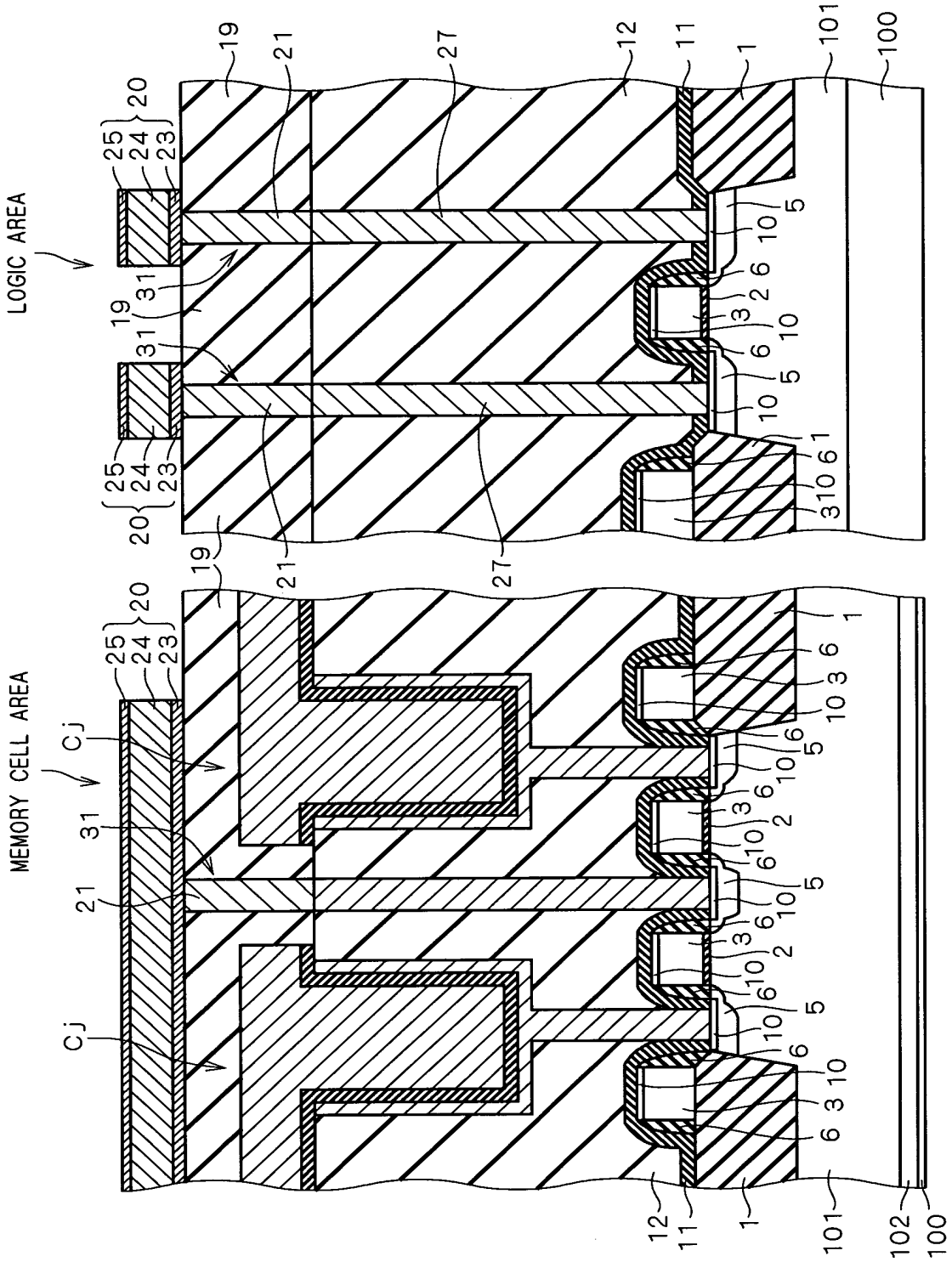
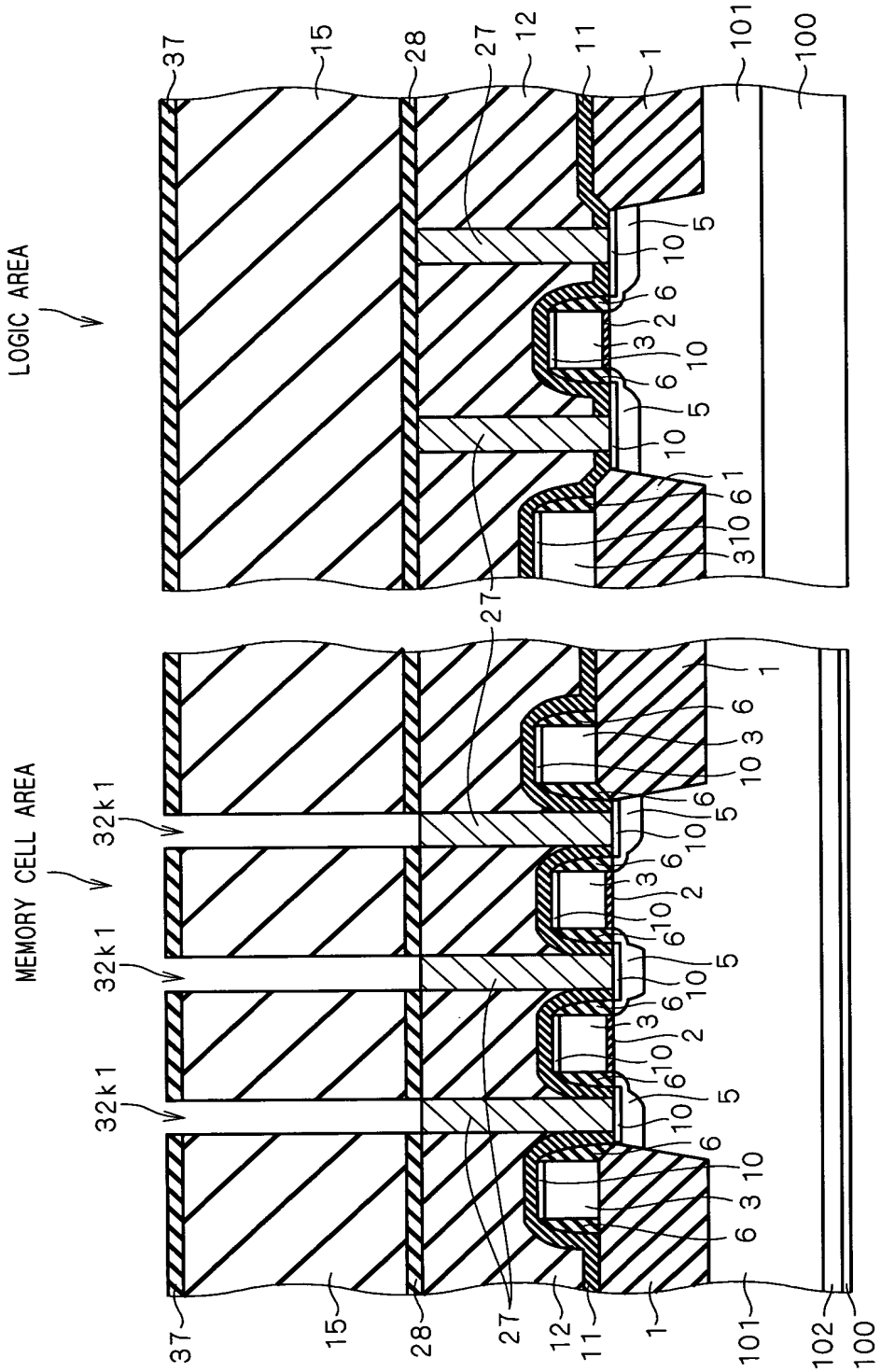

LOGIC AREA
MEMORY CELL AREA
Cj
19
21
27
12
11
1
101
100
102
20
25
24
23
31
10
6
5
3
2

FIG. 70


LOGIC AREA
MEMORY CELL AREA
32k1
32k1
32k1
37
15
28
27
12
11
1
101
102
100

F I G . 7 1

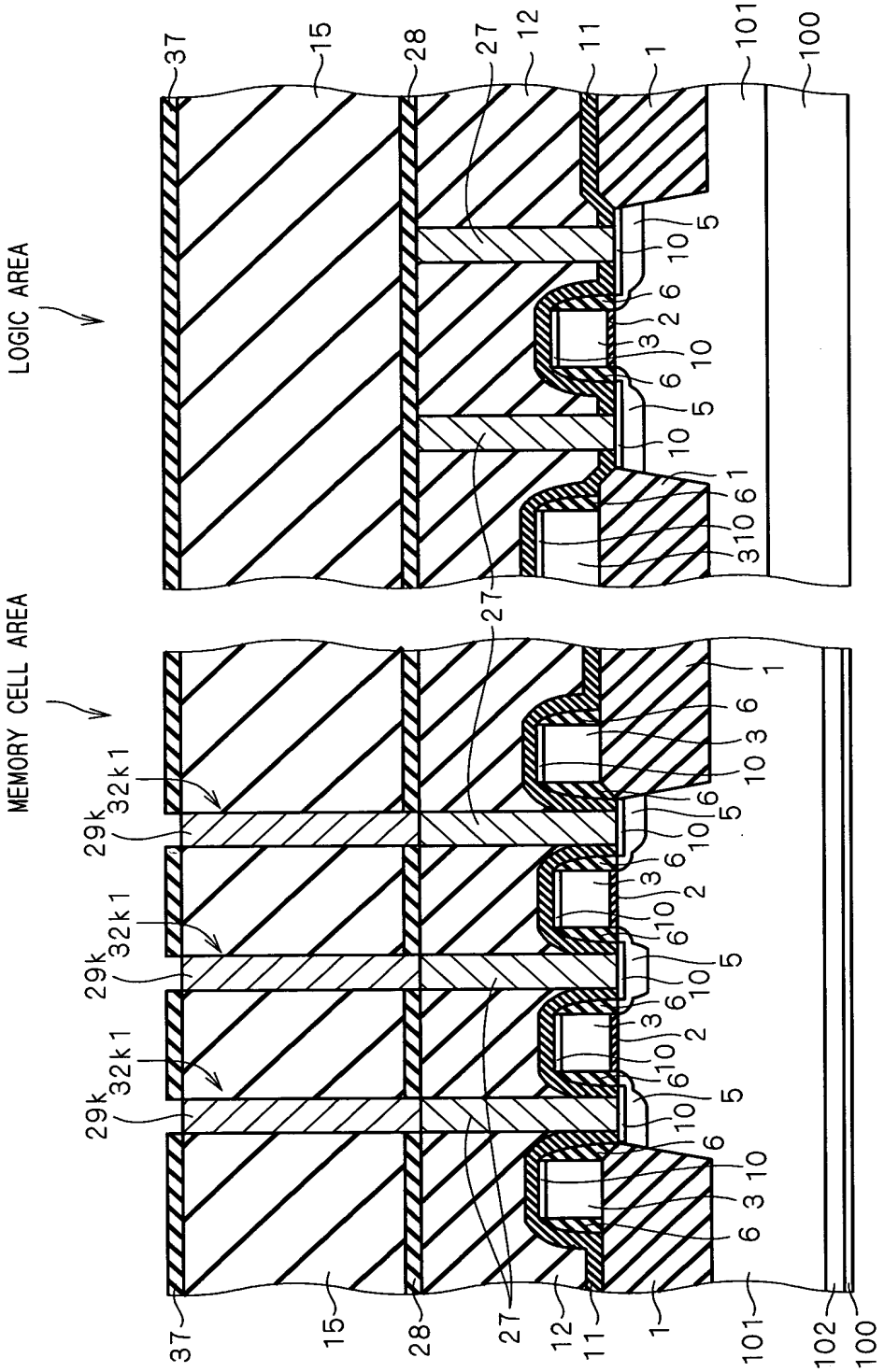

LOGIC AREA
MEMORY CELL AREA
37
15
28
27
12
11
1
101
100
102
29k
32k1
5
10
6
2
3

FIG. 72

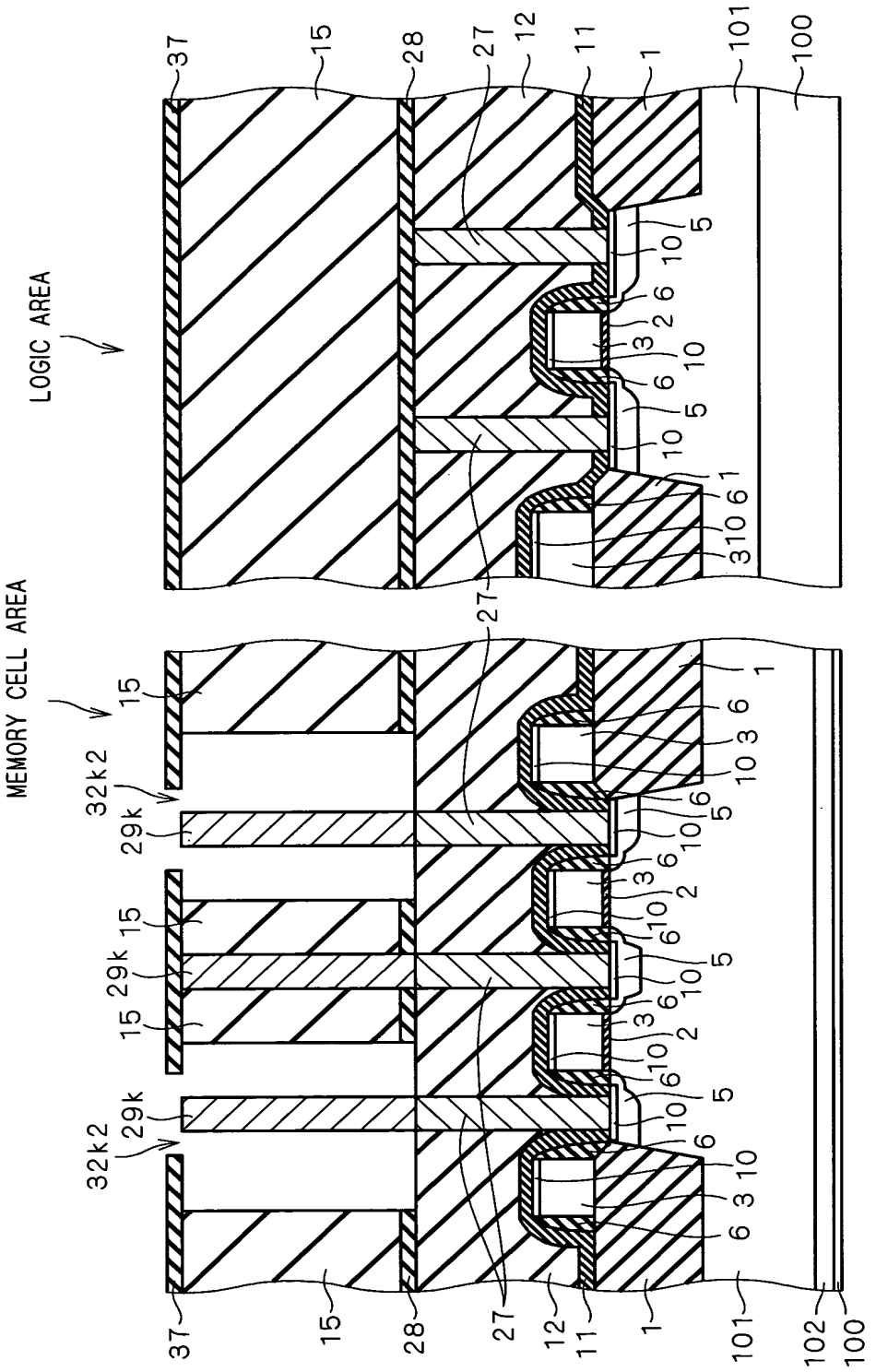

LOGIC AREA
MEMORY CELL AREA
37
15
28
27
12
11
1
101
100
102
32k2
29k
10
6
5
3
2

FIG. 73

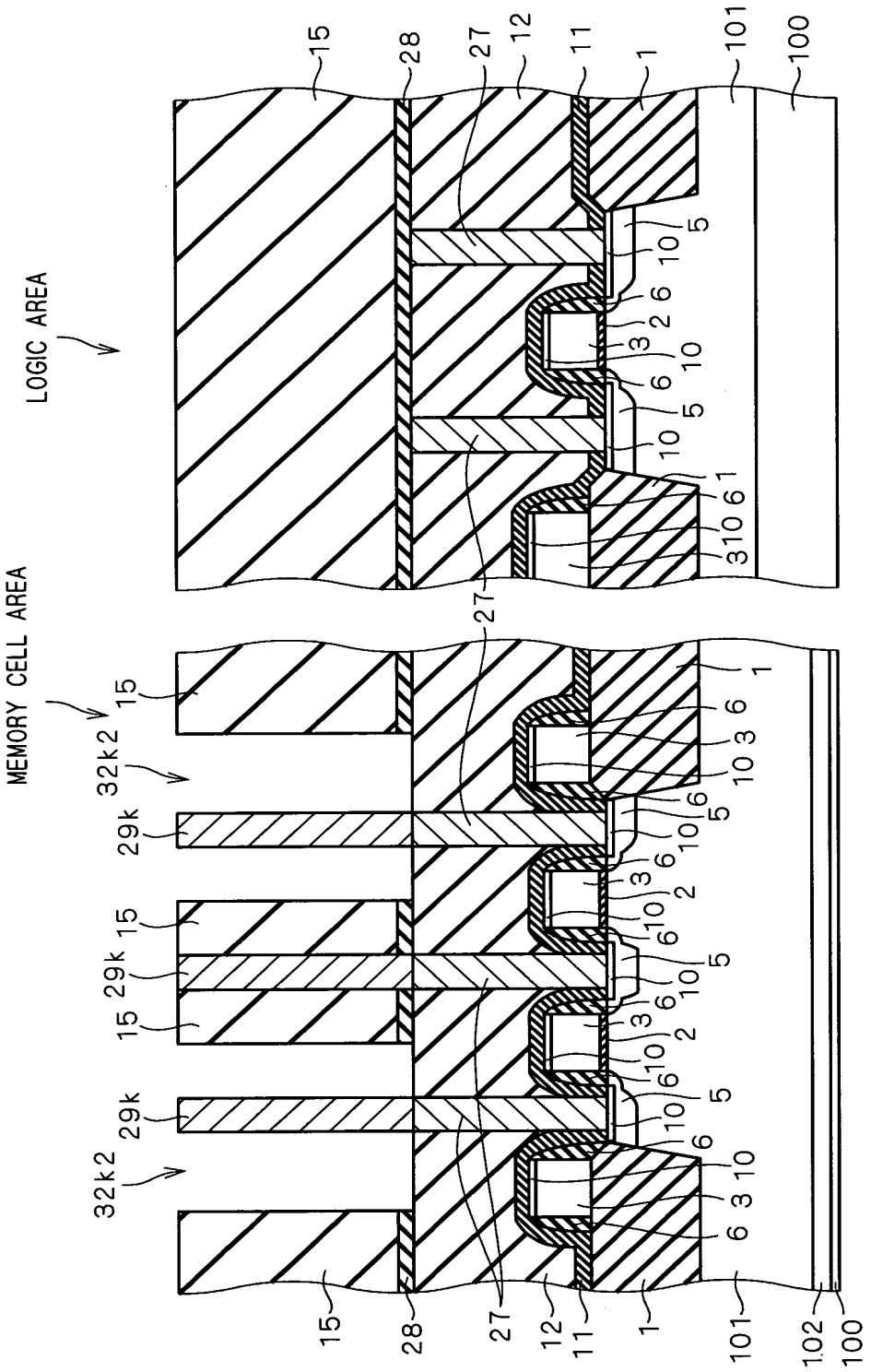

LOGIC AREA
MEMORY CELL AREA
15
28
27
12
11
1
101
100
102
32k2
29k
5
10
6
2
3

FIG. 74

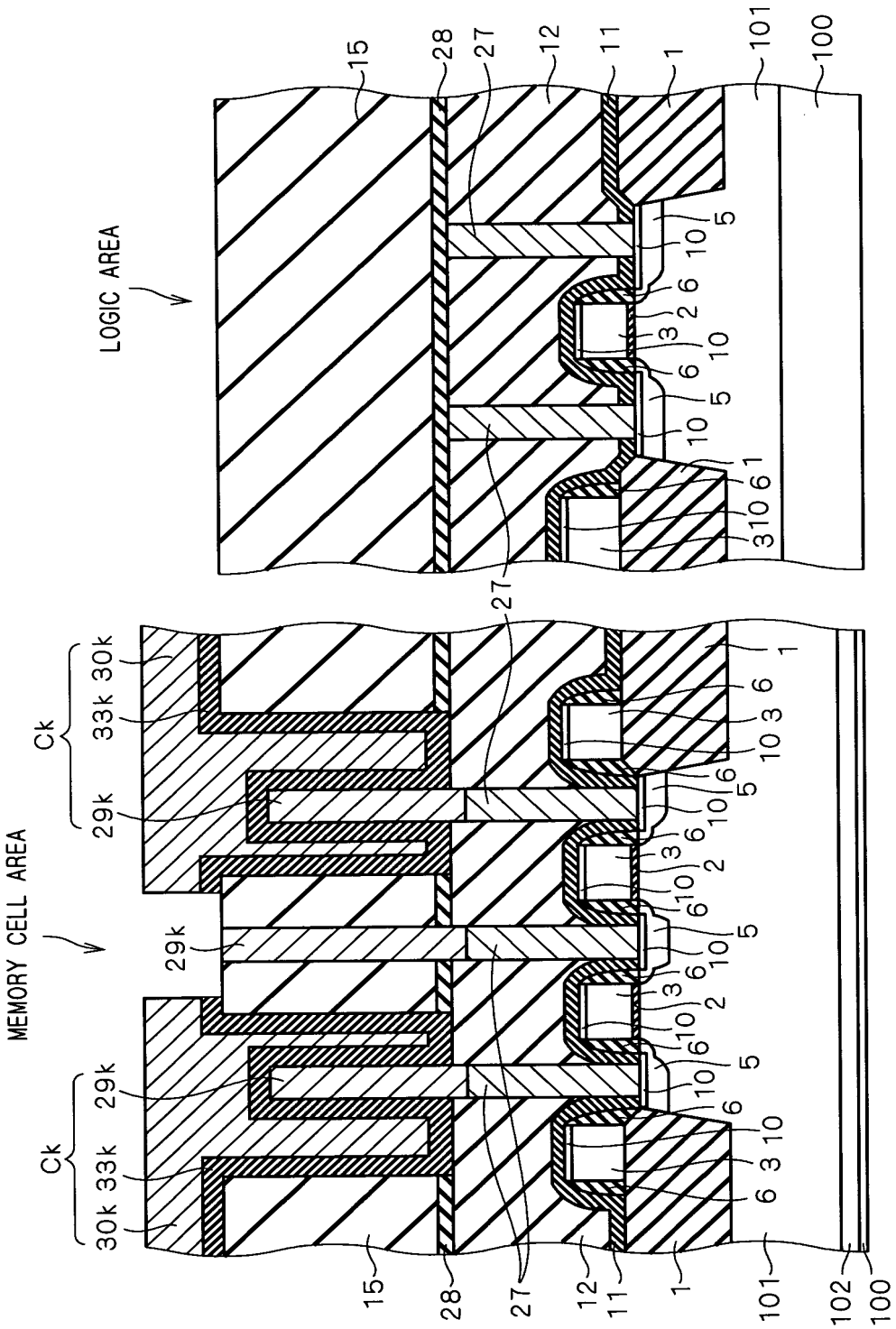

LOGIC AREA
MEMORY CELL AREA
Ck
30k
33k
29k
15
28
27
12
11
1
101
102
100
10
5
6
3
2

FIG. 75

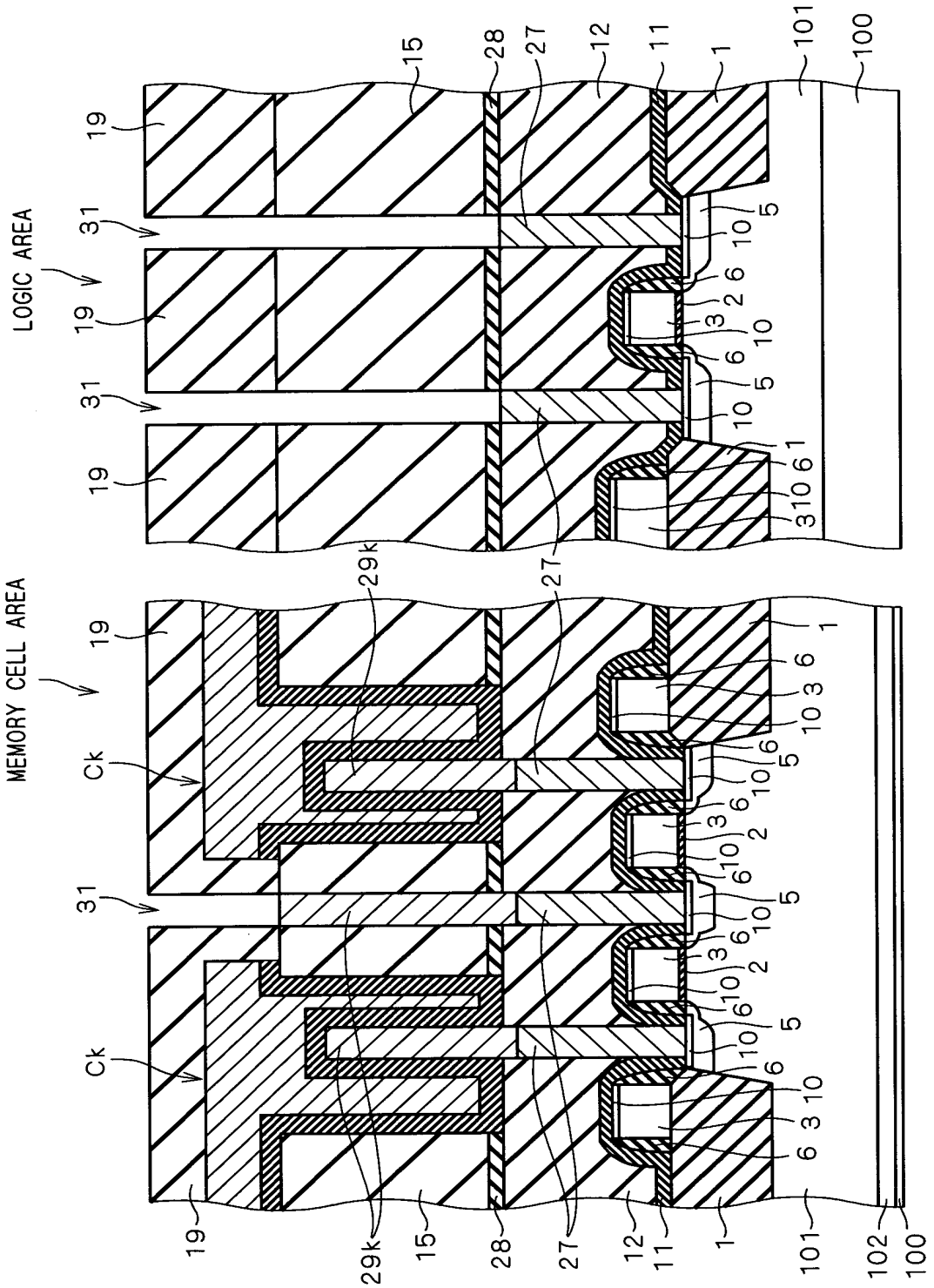

LOGIC AREA
MEMORY CELL AREA
Ck
Ck
19
31
29k
27
15
28
12
11
1
101
102
100
10
6
5
3
2

FIG. 76

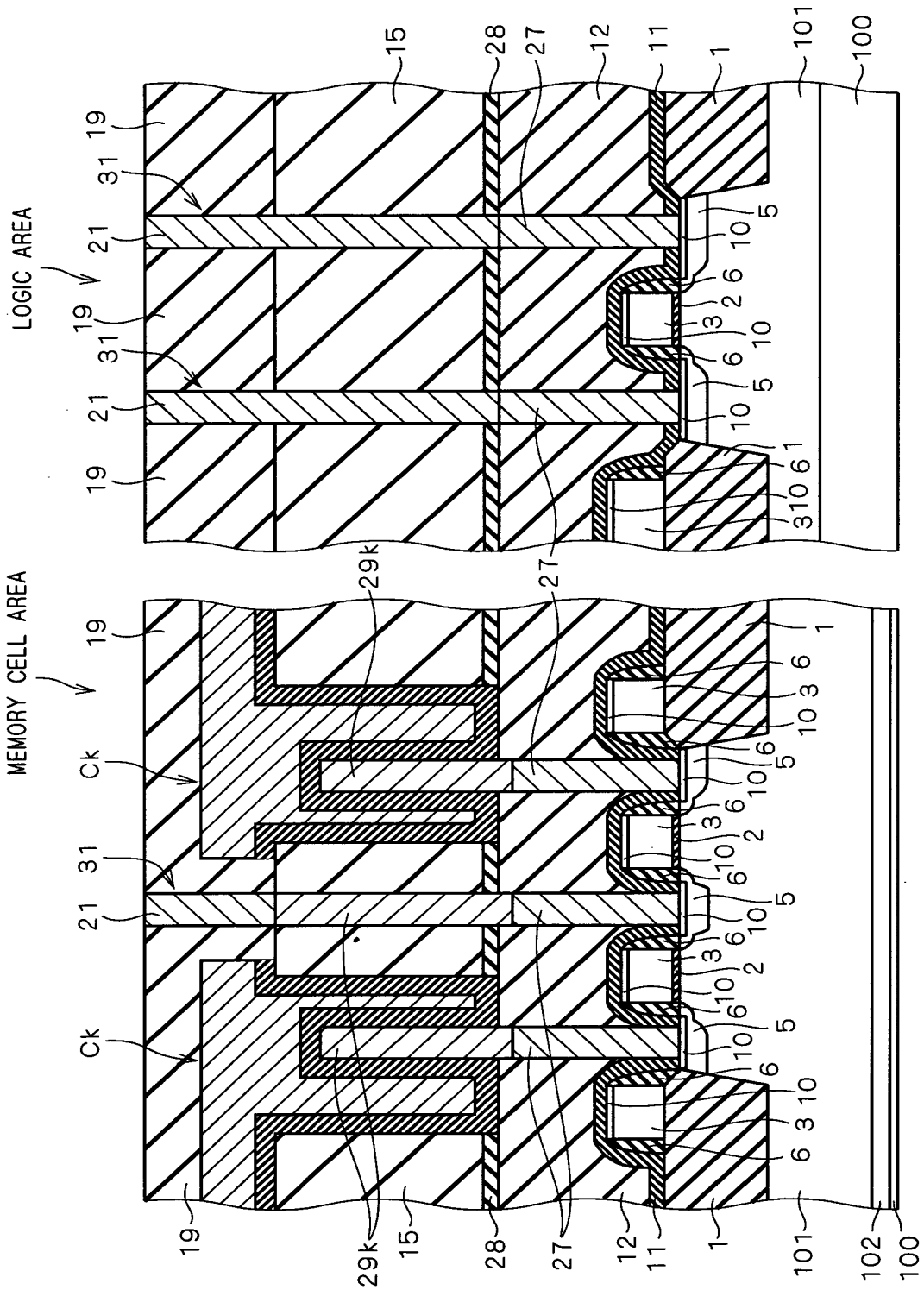

LOGIC AREA
MEMORY CELL AREA
Ck
Ck
19
31
21
29k
27
15
28
12
11
1
101
102
100
5
10
6
3
2

FIG. 77

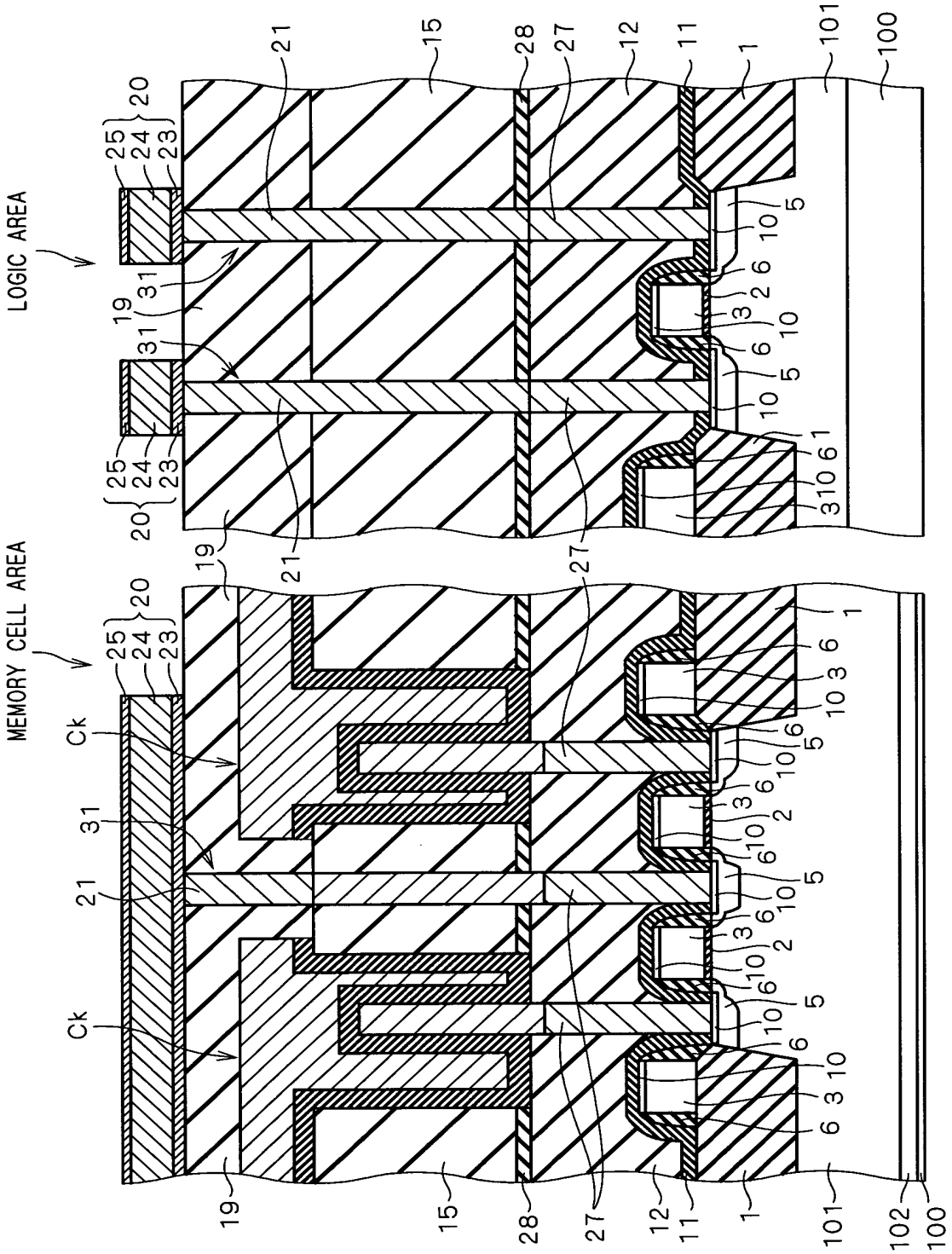

LOGIC AREA
MEMORY CELL AREA
Ck
Ck
19
20
21
23
24
25
27
28
31
100
101
102

FIG. 78

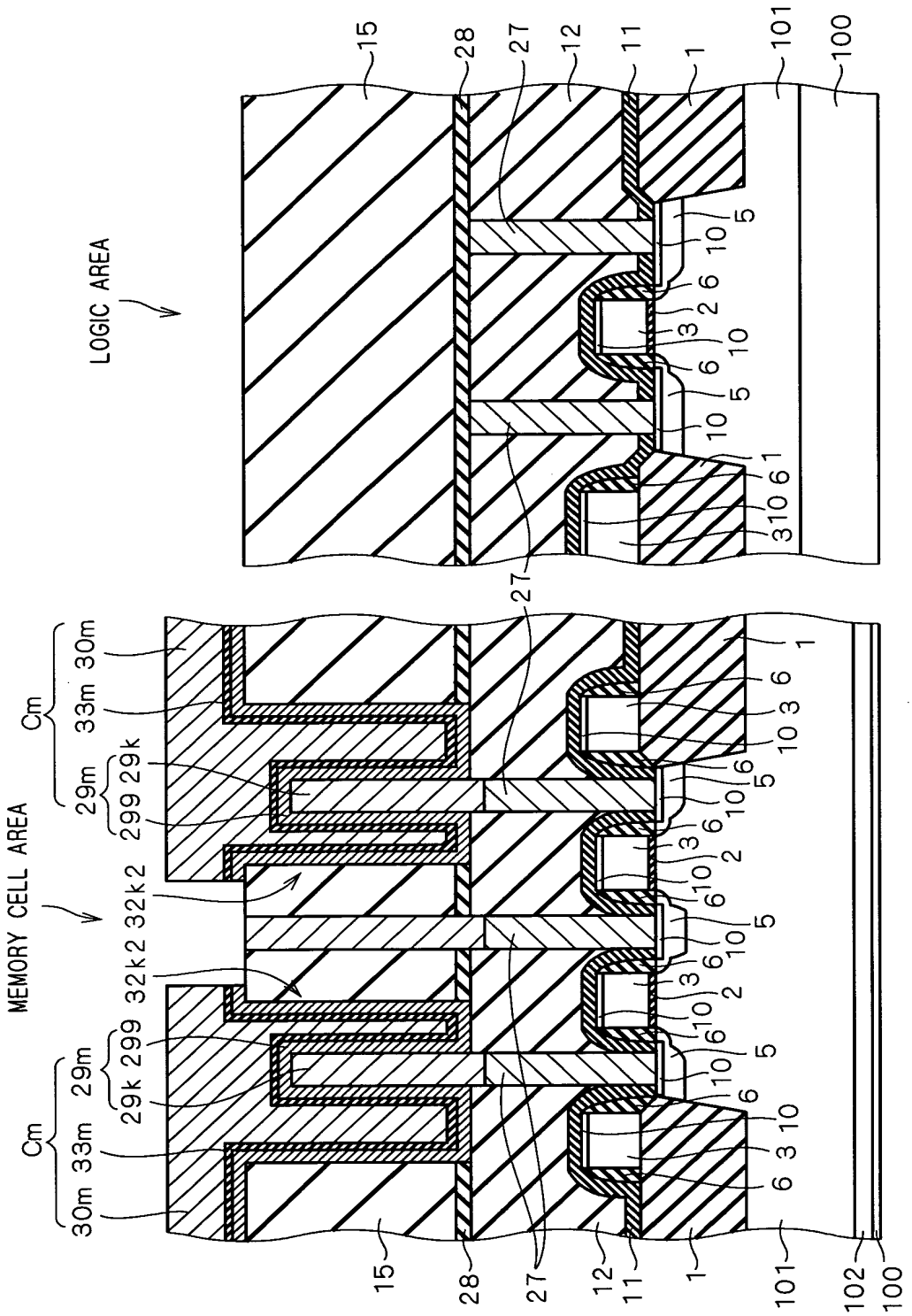

LOGIC AREA
MEMORY CELL AREA
15
28
27
12
11
1
101
100
102
Cm
30m
33m
29m
29k
299
32k2
10
6
5
3
2

FIG. 79

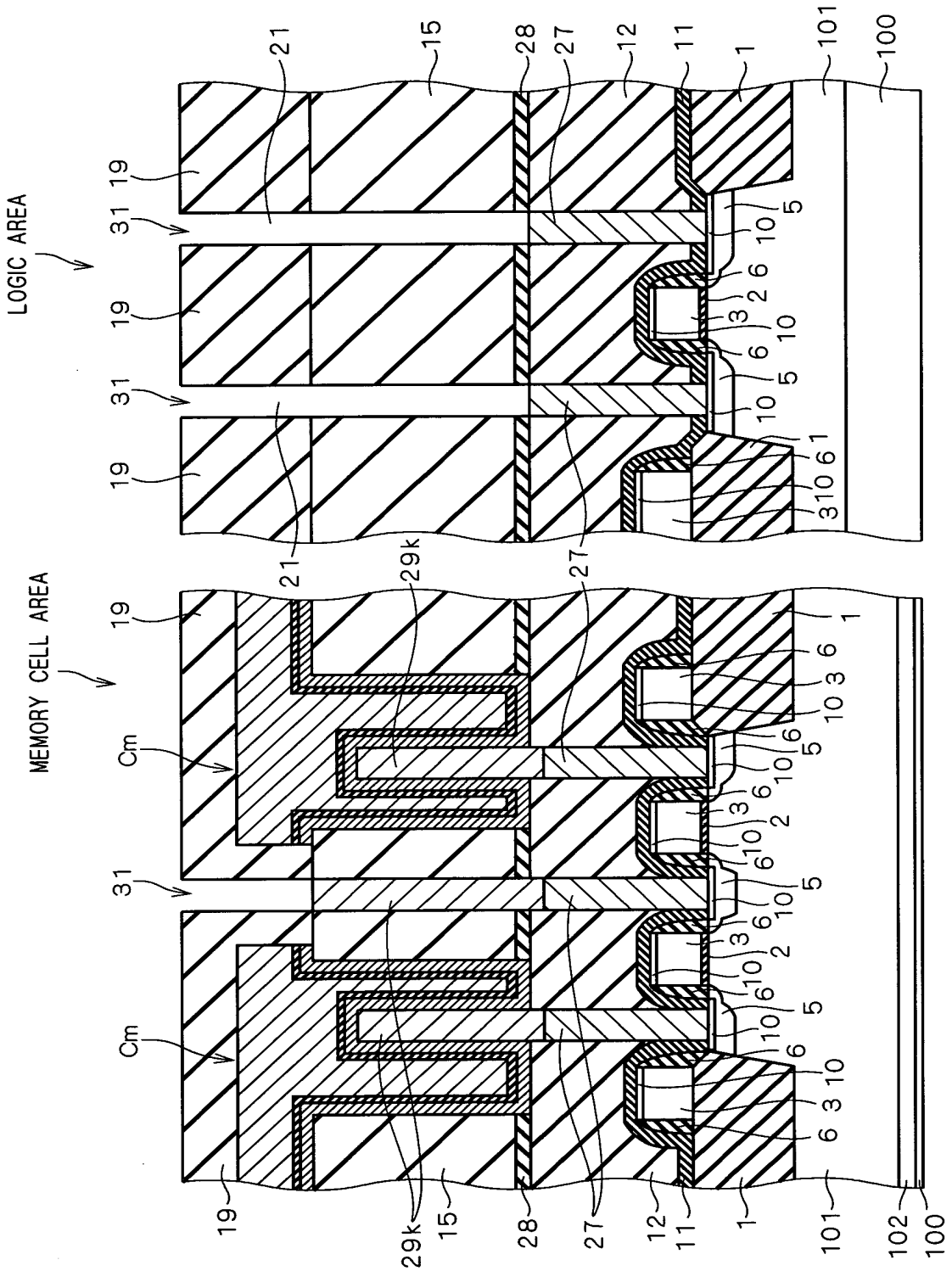

LOGIC AREA
MEMORY CELL AREA
Cm
Cm
19
21
15
28
27
12
11
1
101
100
31
29k
102

FIG. 80

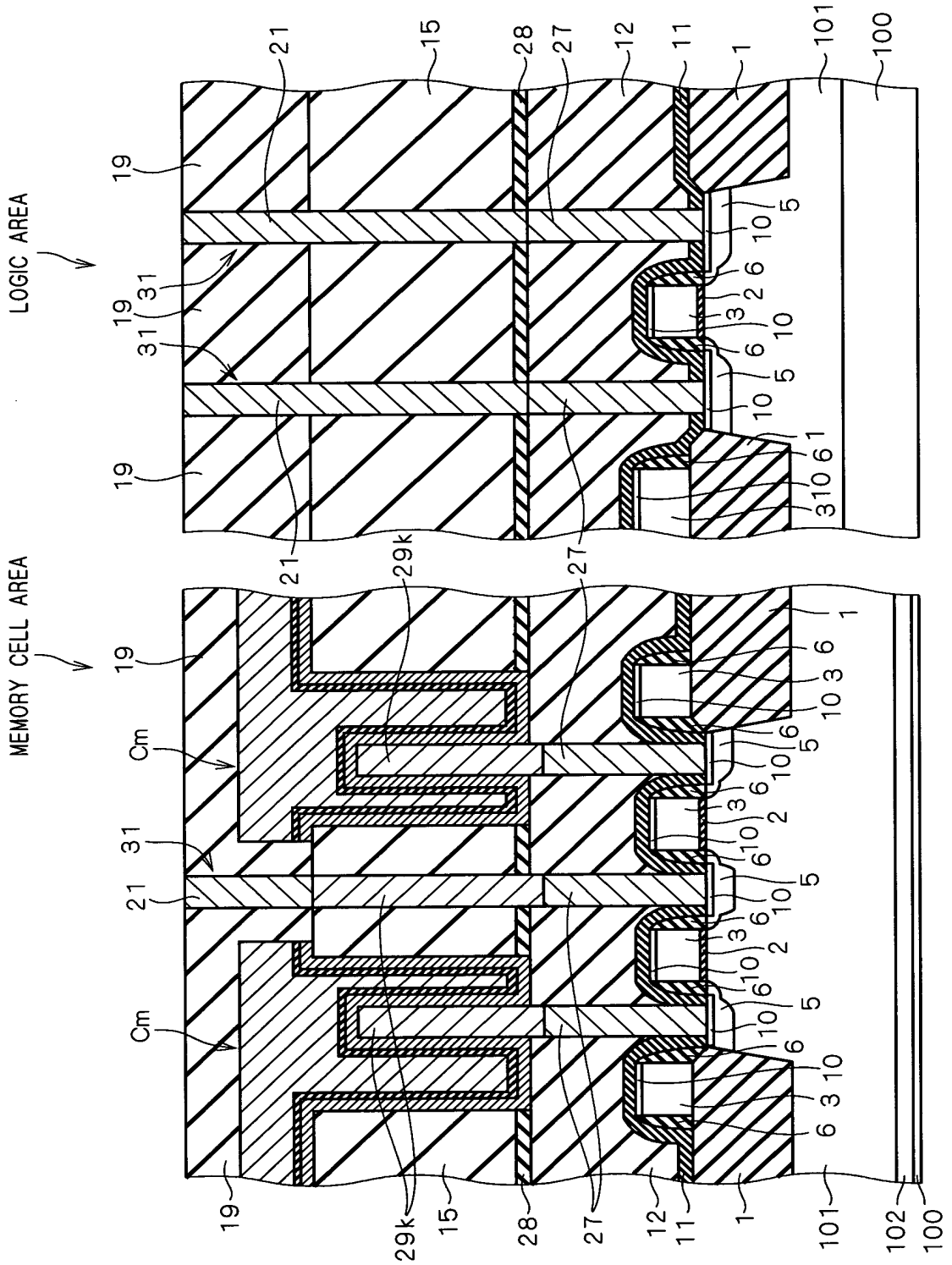

LOGIC AREA
MEMORY CELL AREA
19
21
15
28
27
12
11
1
101
100
31
5
10
6
3
2
Cm
29k
102

FIG. 81

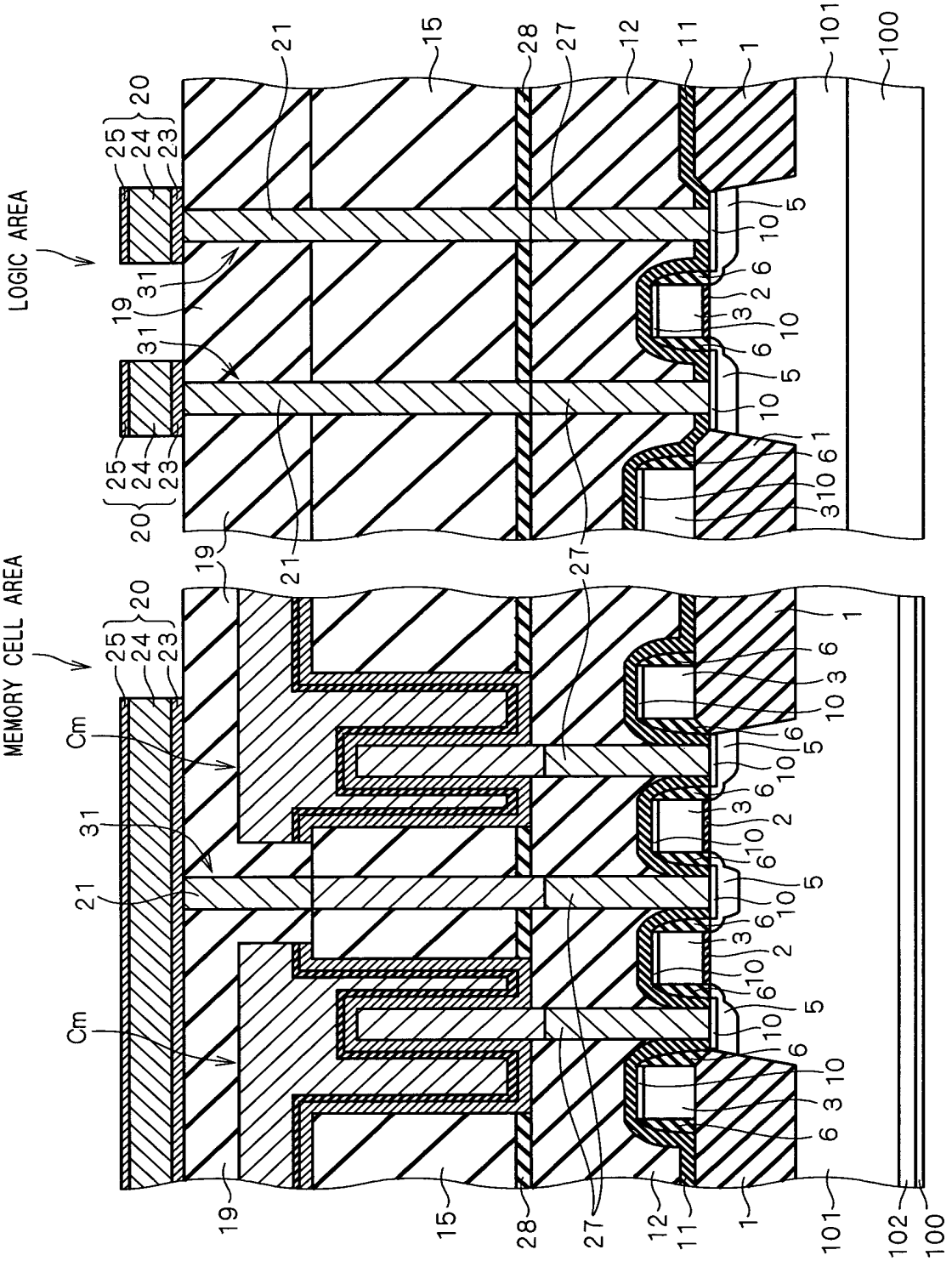

LOGIC AREA
MEMORY CELL AREA
Cm
Cm
19
21
15
28
27
12
11
1
101
102
100
20
23
24
25
31
10
6
5
3
2

FIG. 82

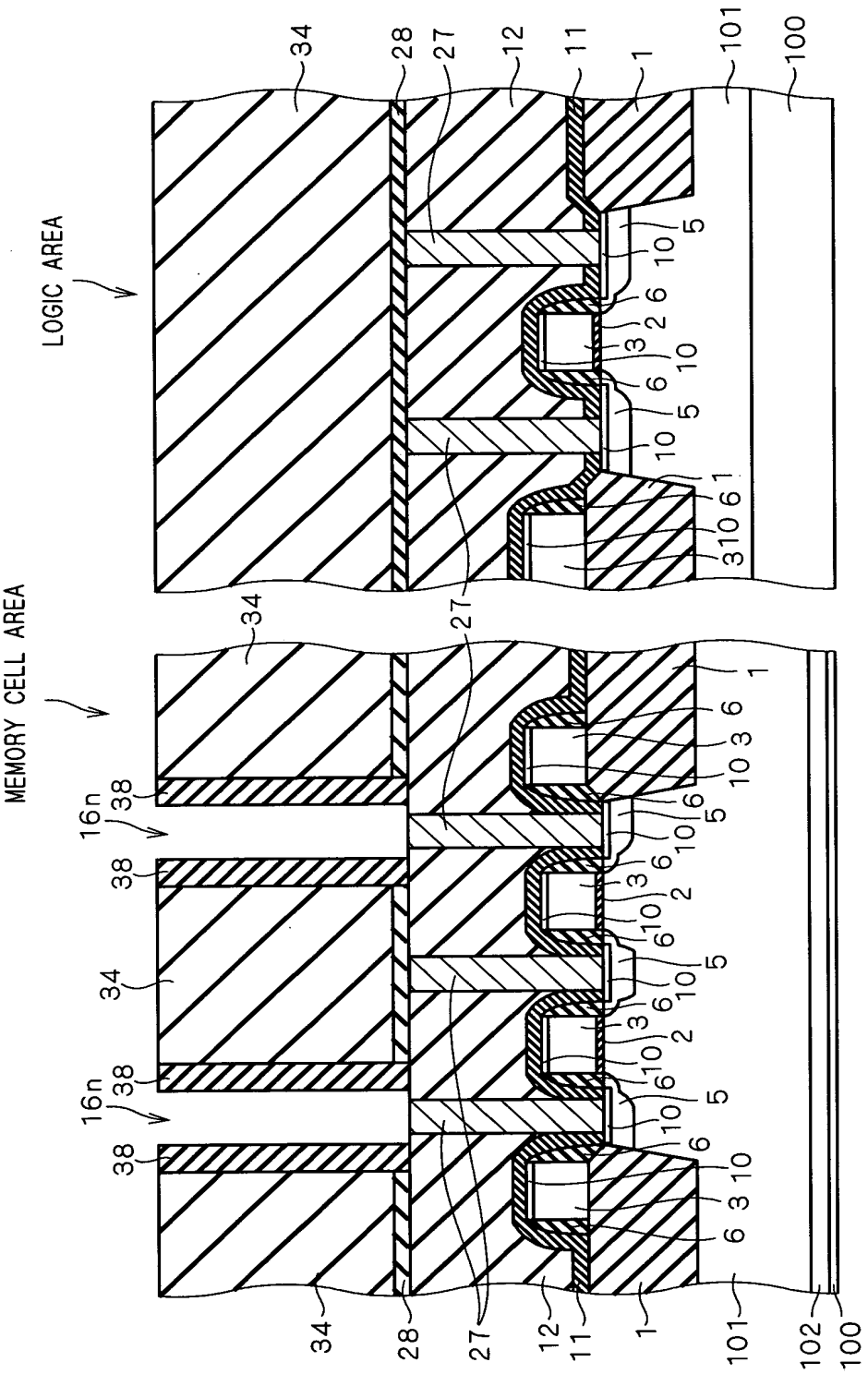

LOGIC AREA
MEMORY CELL AREA
34
28
27
12
11
1
101
100
102
38
16n
10
6
5
3
2

FIG. 83

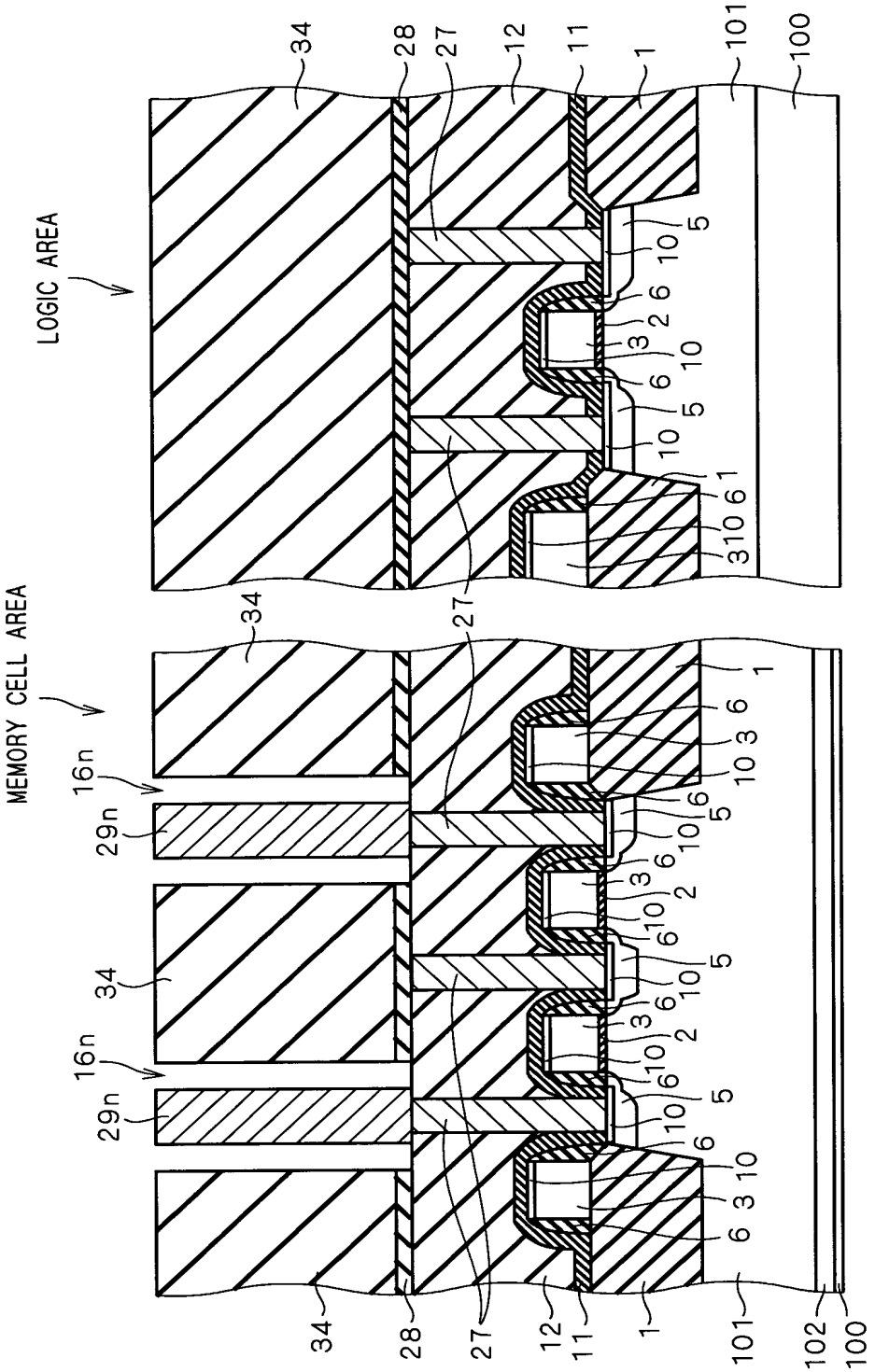

LOGIC AREA
MEMORY CELL AREA
34
28
27
12
11
1
101
100
102
16n
29n
10
6
5
3
2

FIG. 84

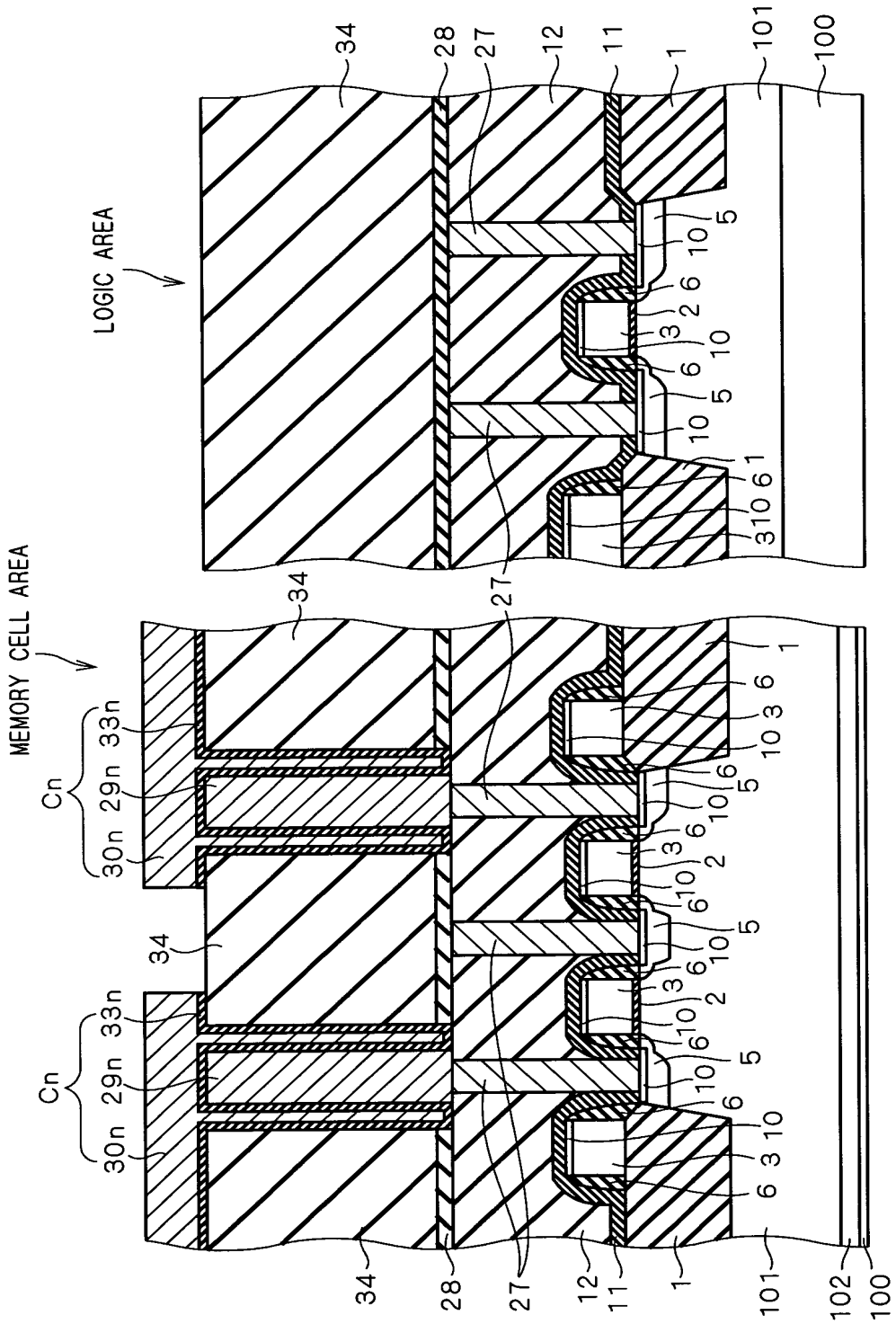

LOGIC AREA
MEMORY CELL AREA
Cn
30n
29n
33n
34
28
27
12
11
1
101
102
100
10
5
6
3
2

FIG. 85

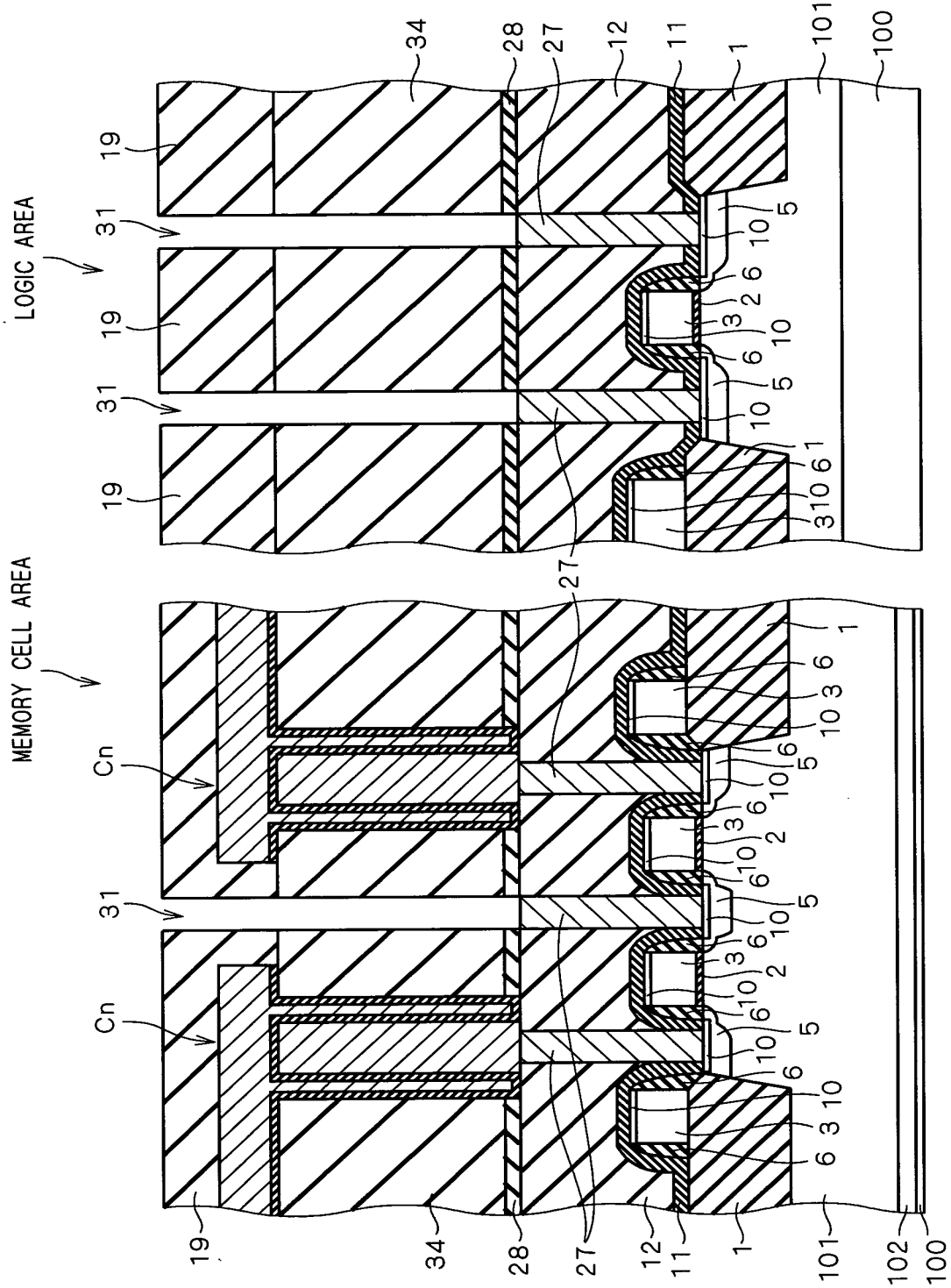

LOGIC AREA
MEMORY CELL AREA
Cn
Cn
19
31
19
31
19
34
28
27
12
11
1
101
100
102

FIG. 86

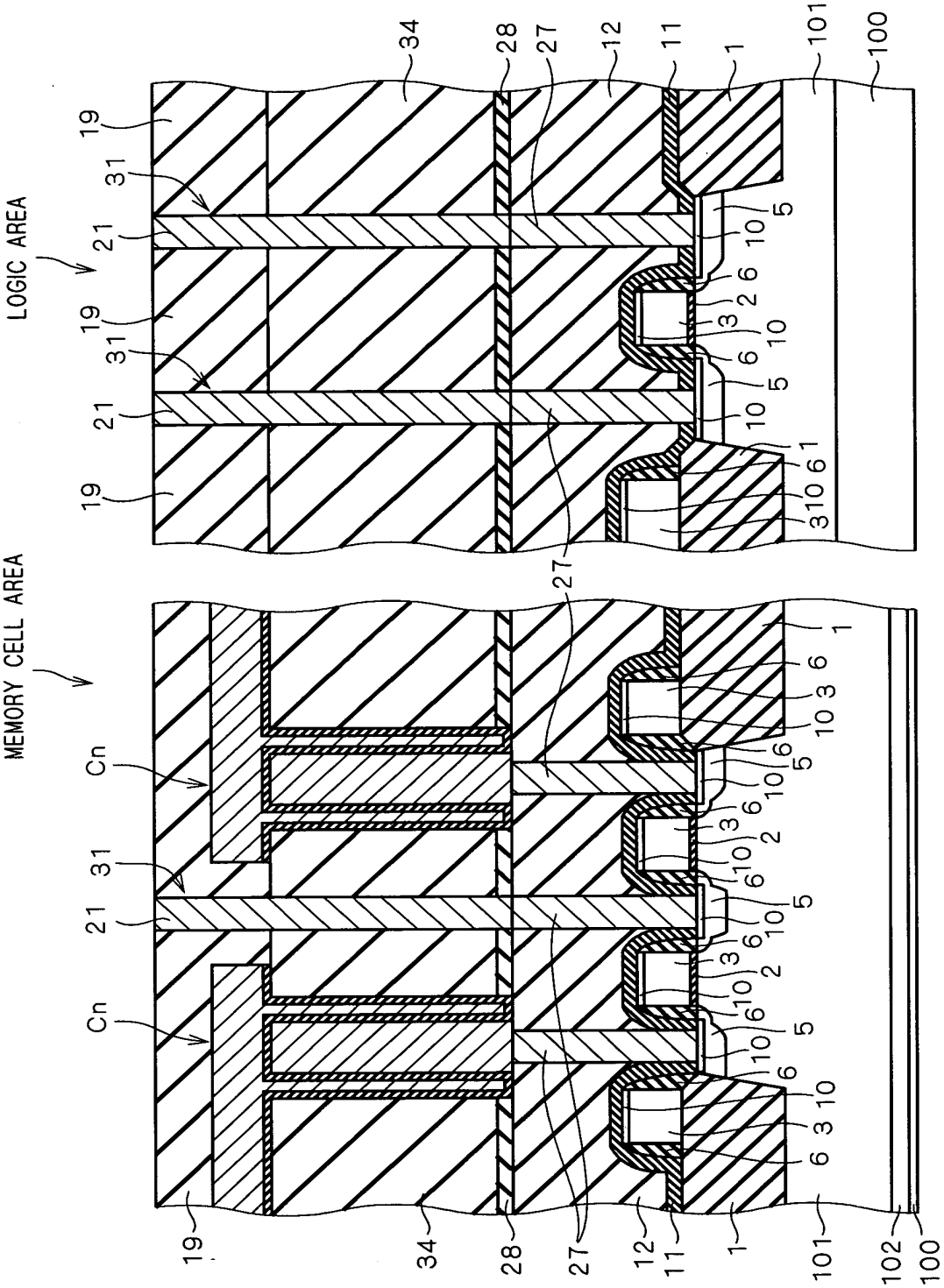
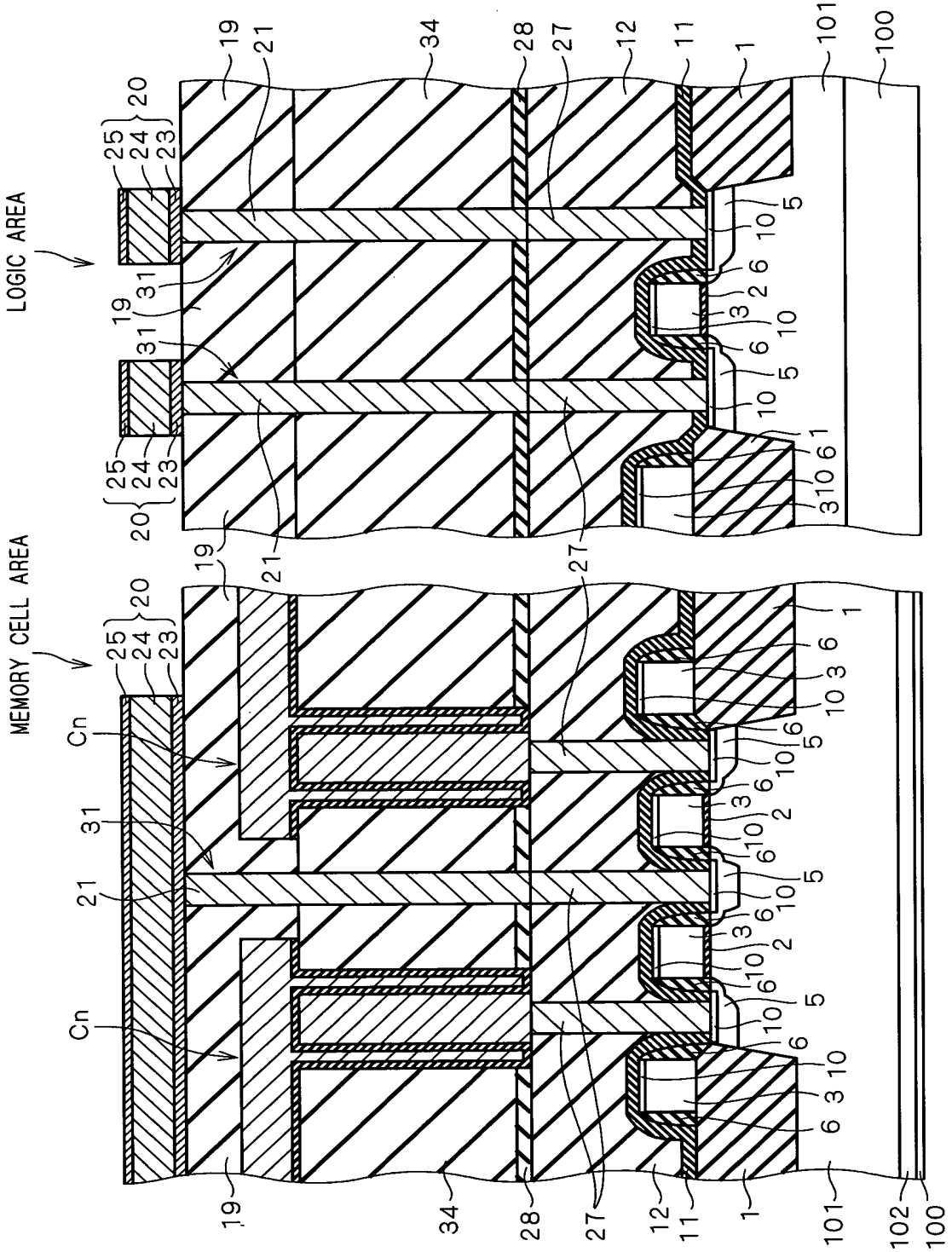

LOGIC AREA
MEMORY CELL AREA
Cn
Cn
19
31
21
34
28
27
12
11
1
101
100
102

FIG. 87


LOGIC AREA
MEMORY CELL AREA
Cn
Cn
19
21
34
28
27
12
11
1
101
100
102
20
23
24
25
31
5
6
10
2
3

F I G . 8 8

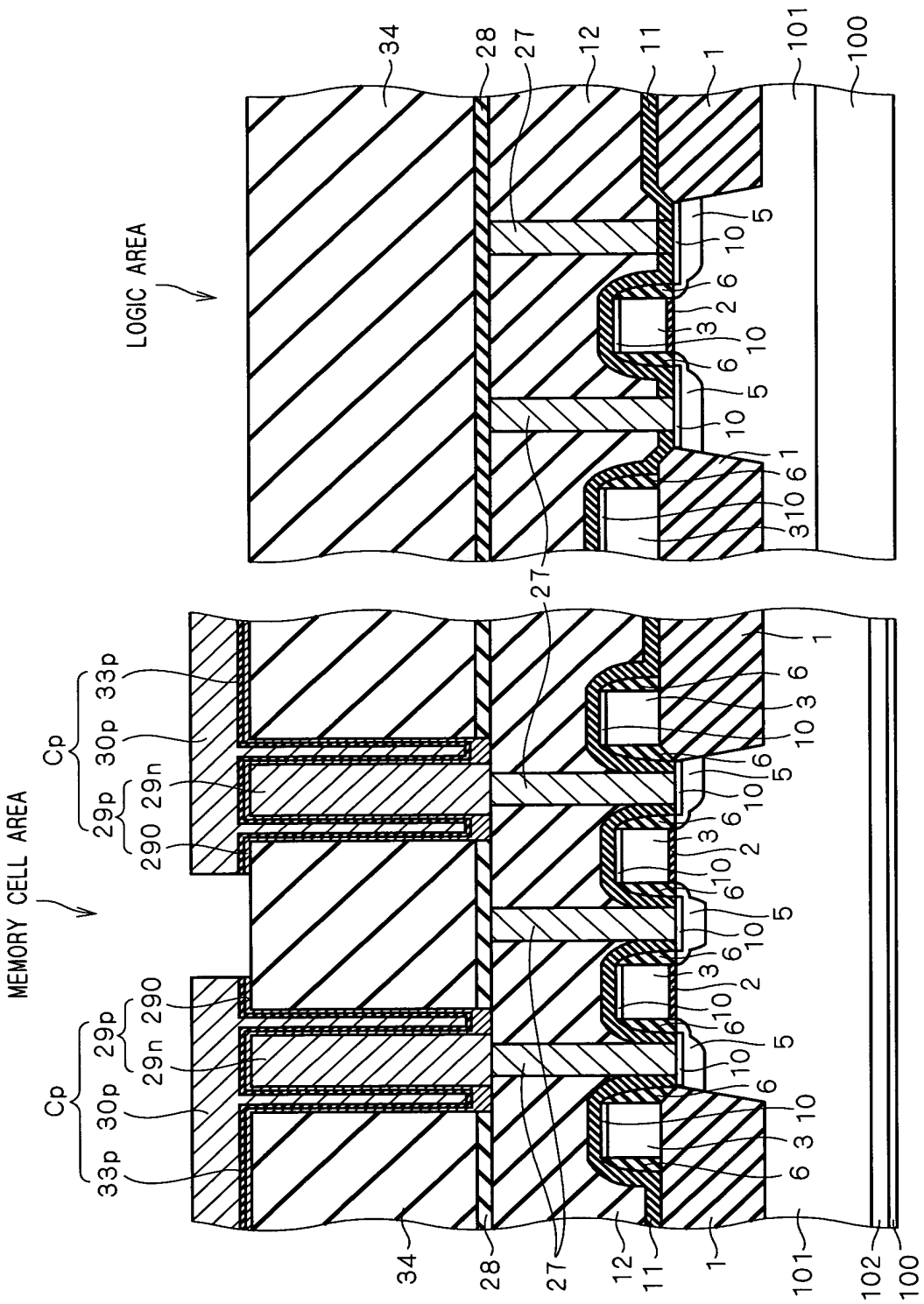

LOGIC AREA
MEMORY CELL AREA
Cp
33p
30p
29p
29n
290
34
28
27
12
11
1
101
102
100
5
10
6
3
2

FIG. 89

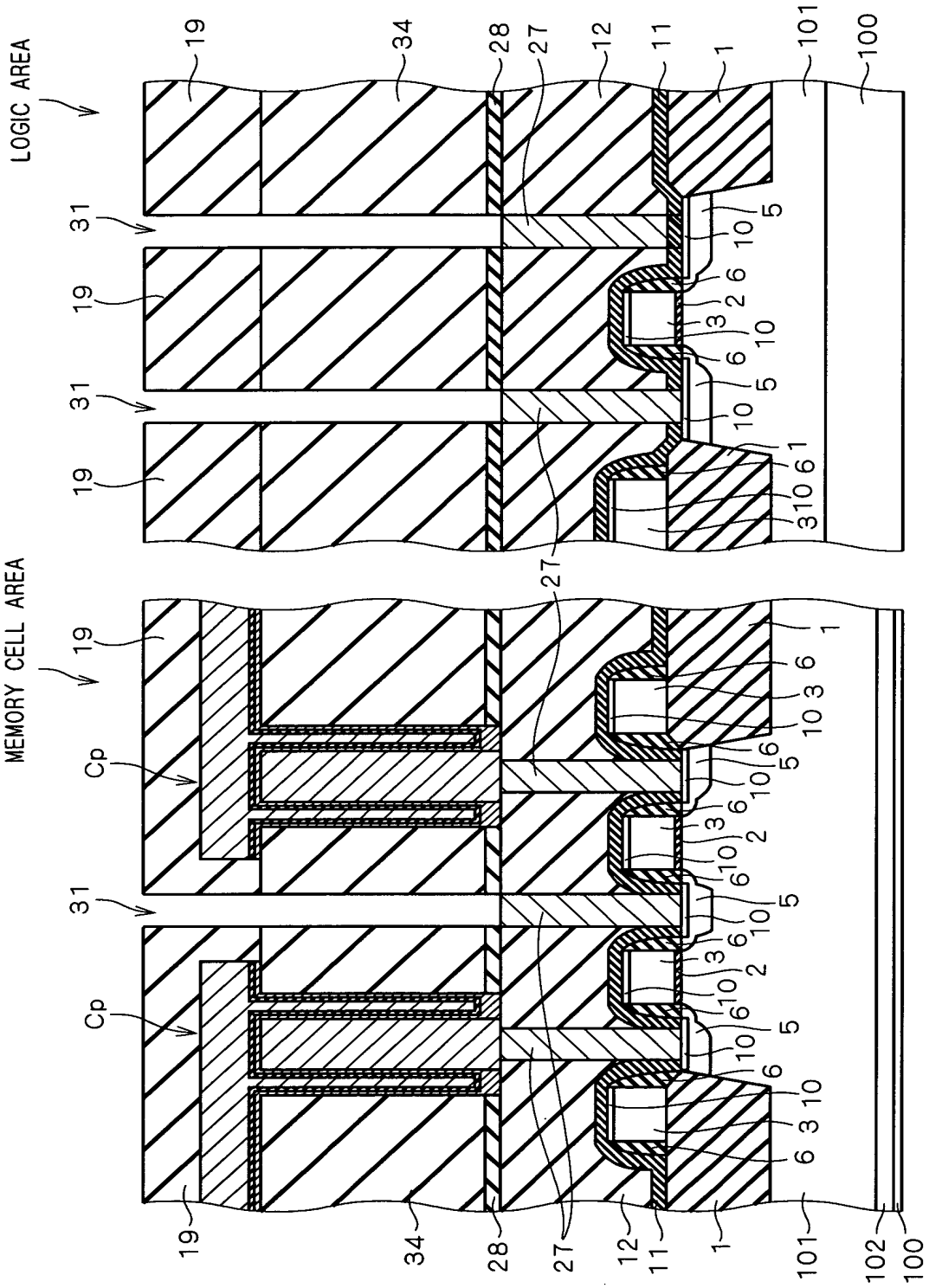

LOGIC AREA
MEMORY CELL AREA
19
34
28
27
12
11
1
101
100
31
5
10
6
2
3
Cp
102

FIG. 90

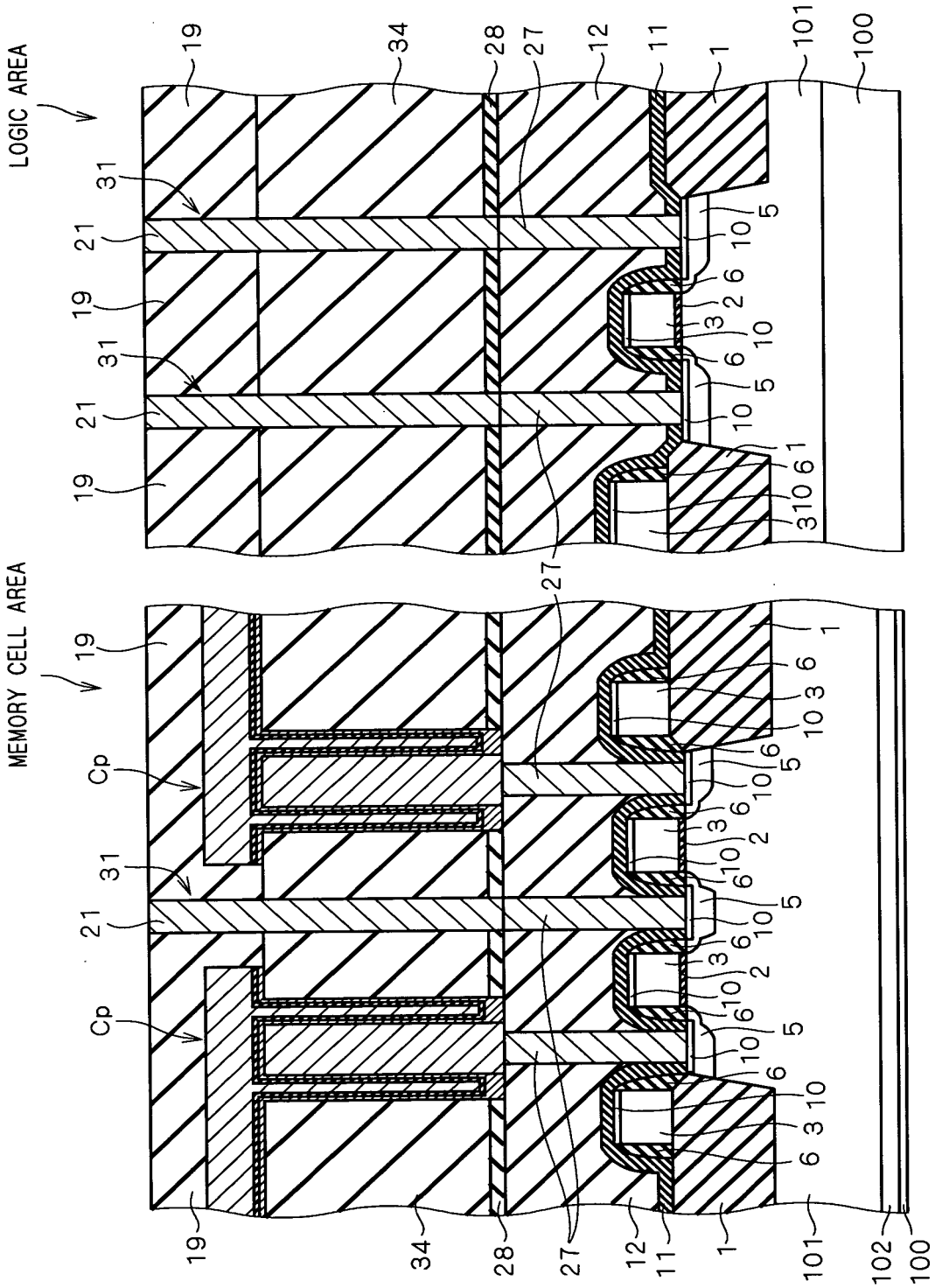

LOGIC AREA
MEMORY CELL AREA
19
34
28
27
12
11
1
101
100
31
21
5
10
6
2
3
Cp
102

FIG. 91

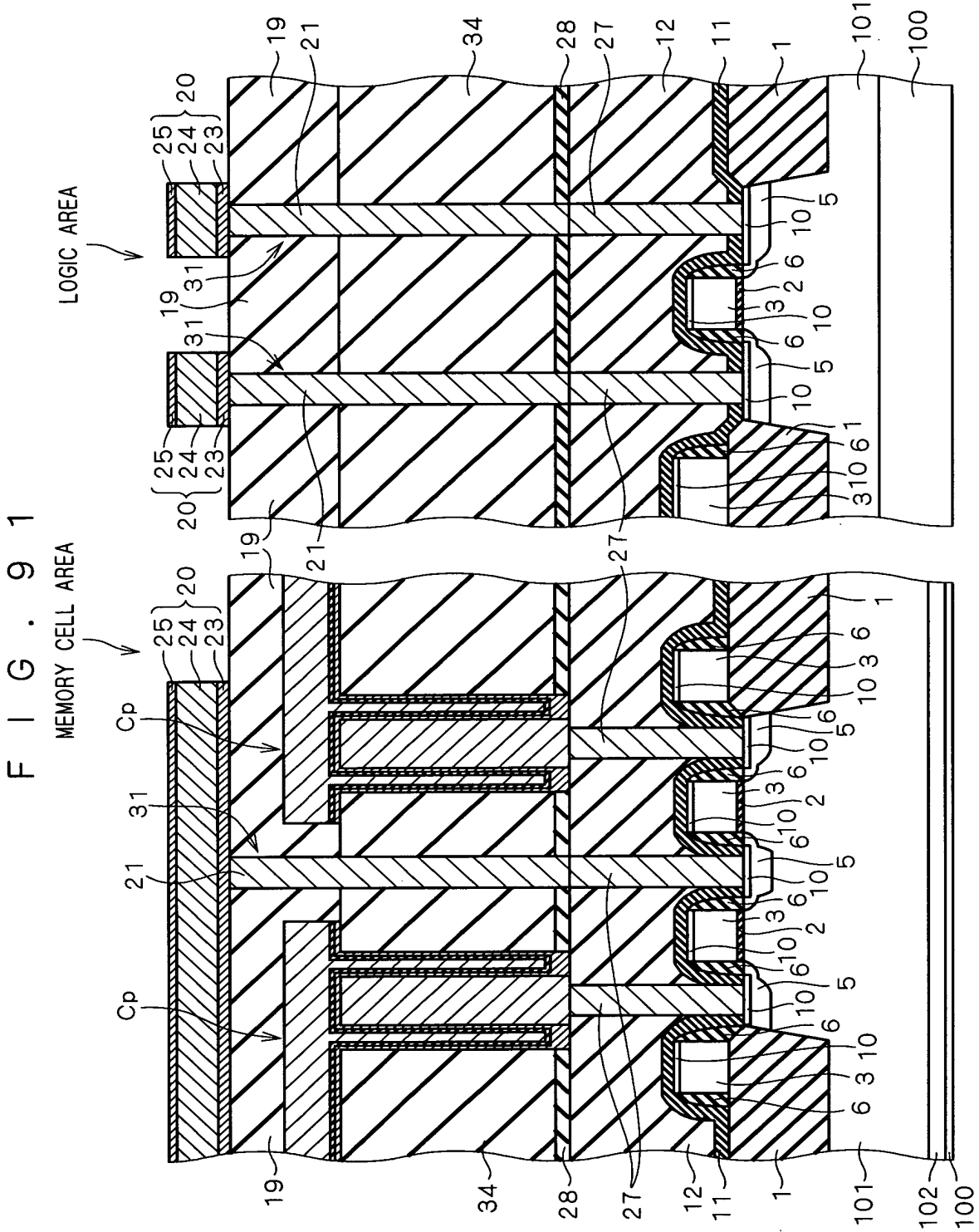

LOGIC AREA
MEMORY CELL AREA
Cp
Cp
19
21
31
20
23
24
25
34
28
27
12
11
1
101
102
100
2
3
5
6
10

FIG. 92

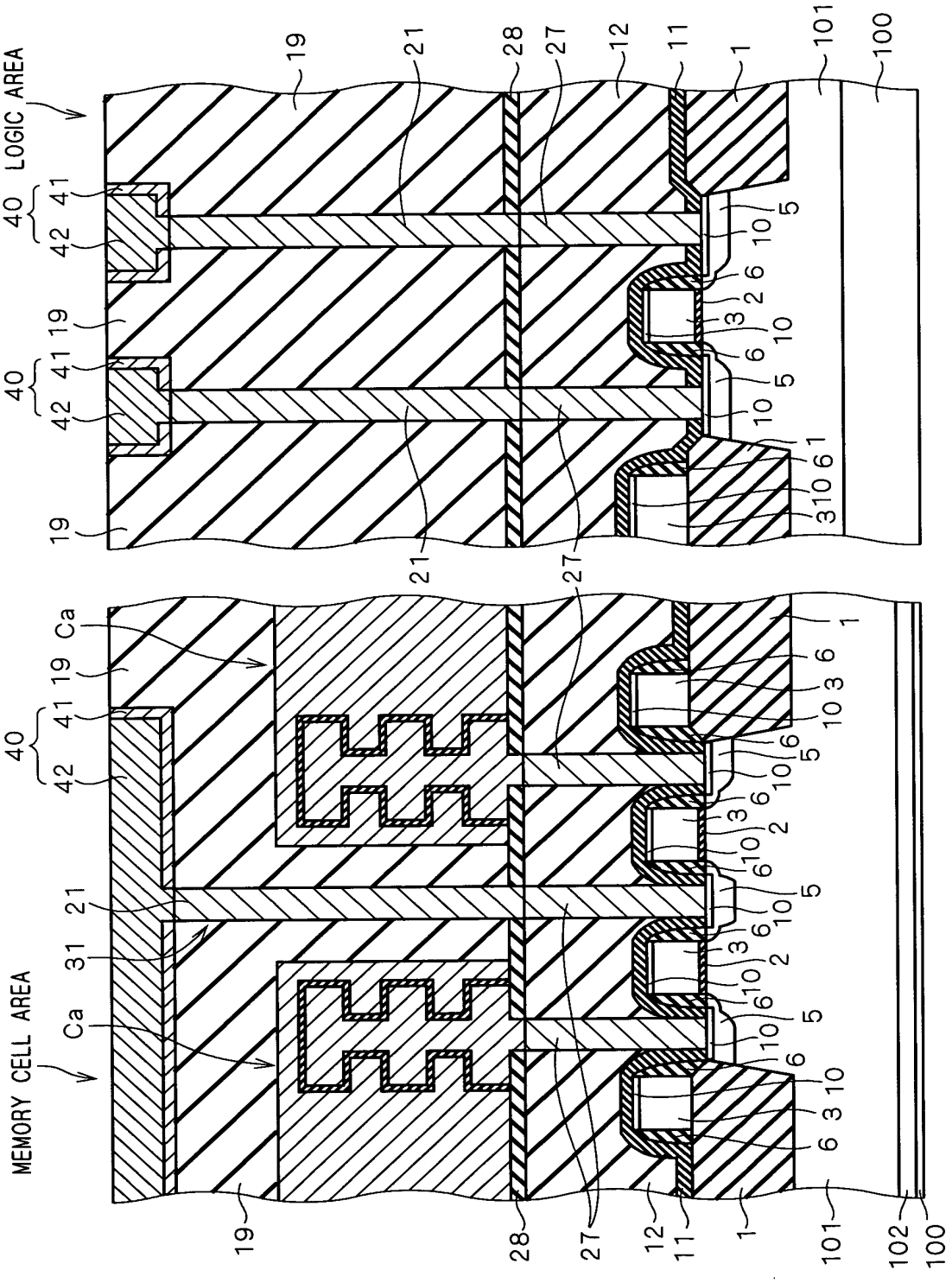

LOGIC AREA
MEMORY CELL AREA
Ca
19
21
28
27
12
11
1
101
100
102
40
41
42
31
10
6
5
3
2

FIG. 93

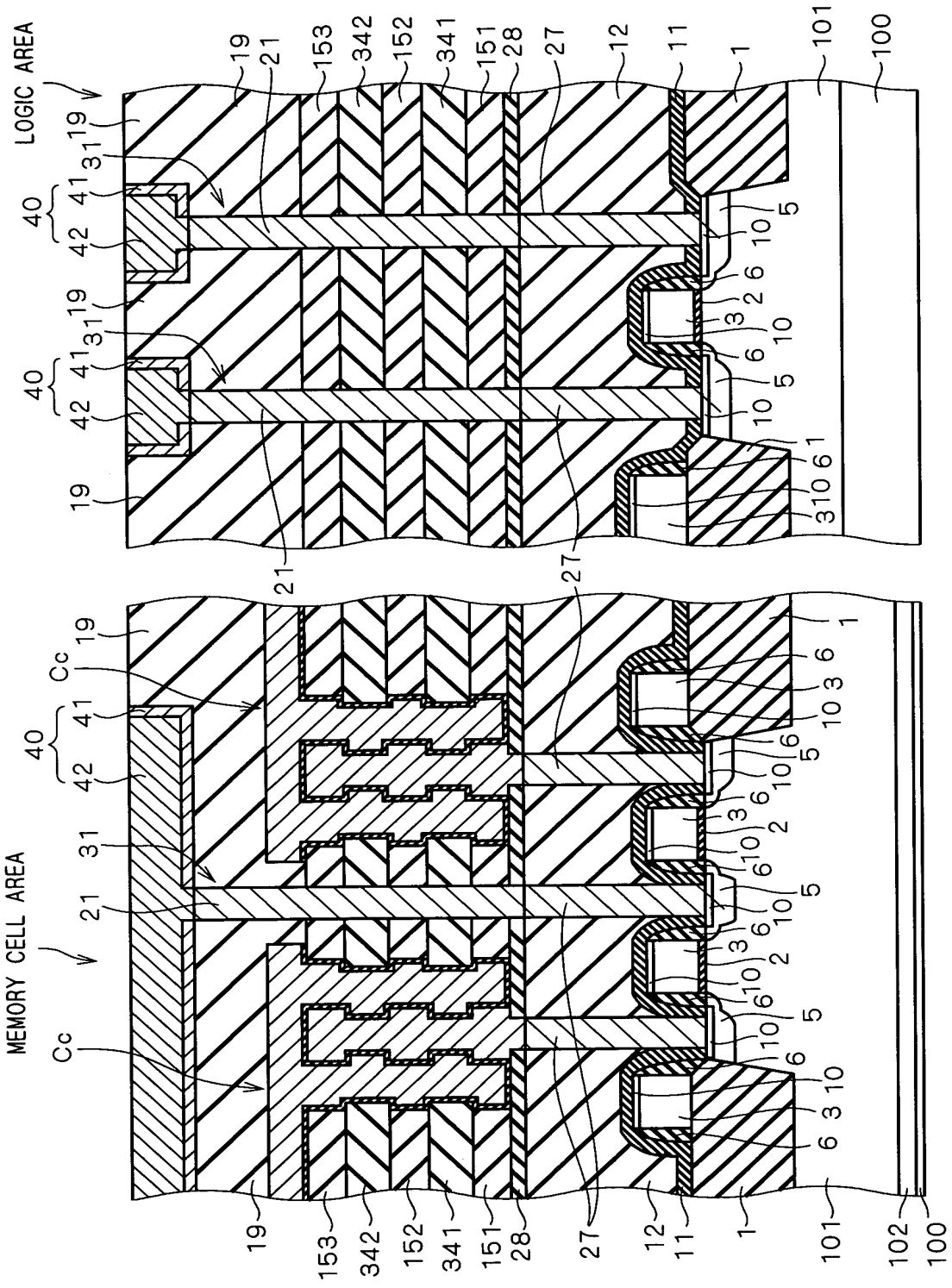

LOGIC AREA
MEMORY CELL AREA
Cc
19
21
153
342
152
341
151
28
27
12
11
1
101
100
102
40
41
42
31
5
10
6
3
2

FIG. 94

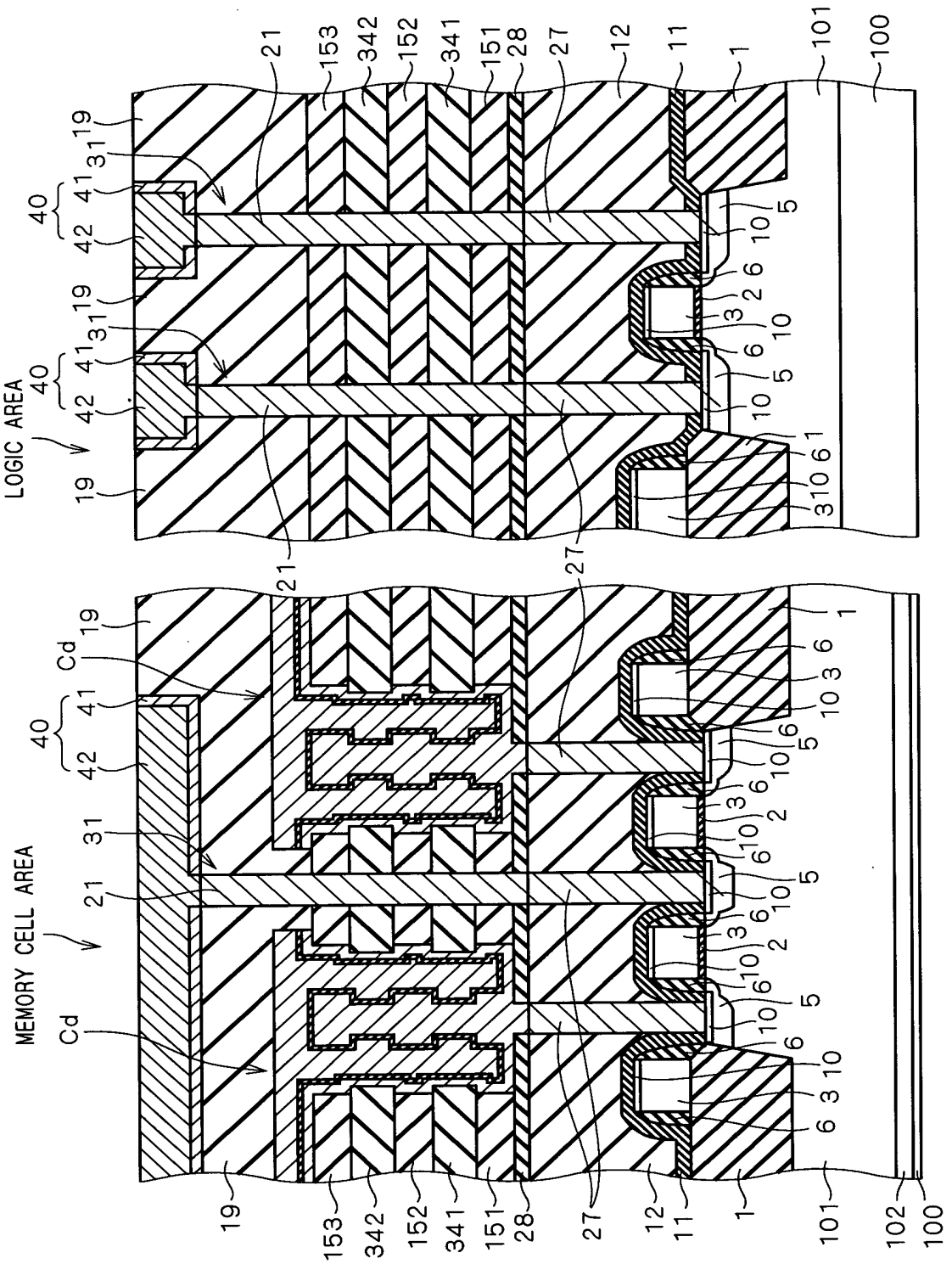

LOGIC AREA
MEMORY CELL AREA
Cd
19
21
153
342
152
341
151
28
27
12
11
1
101
100
102
40
41
42
31
5
10
6
3
2

FIG. 95

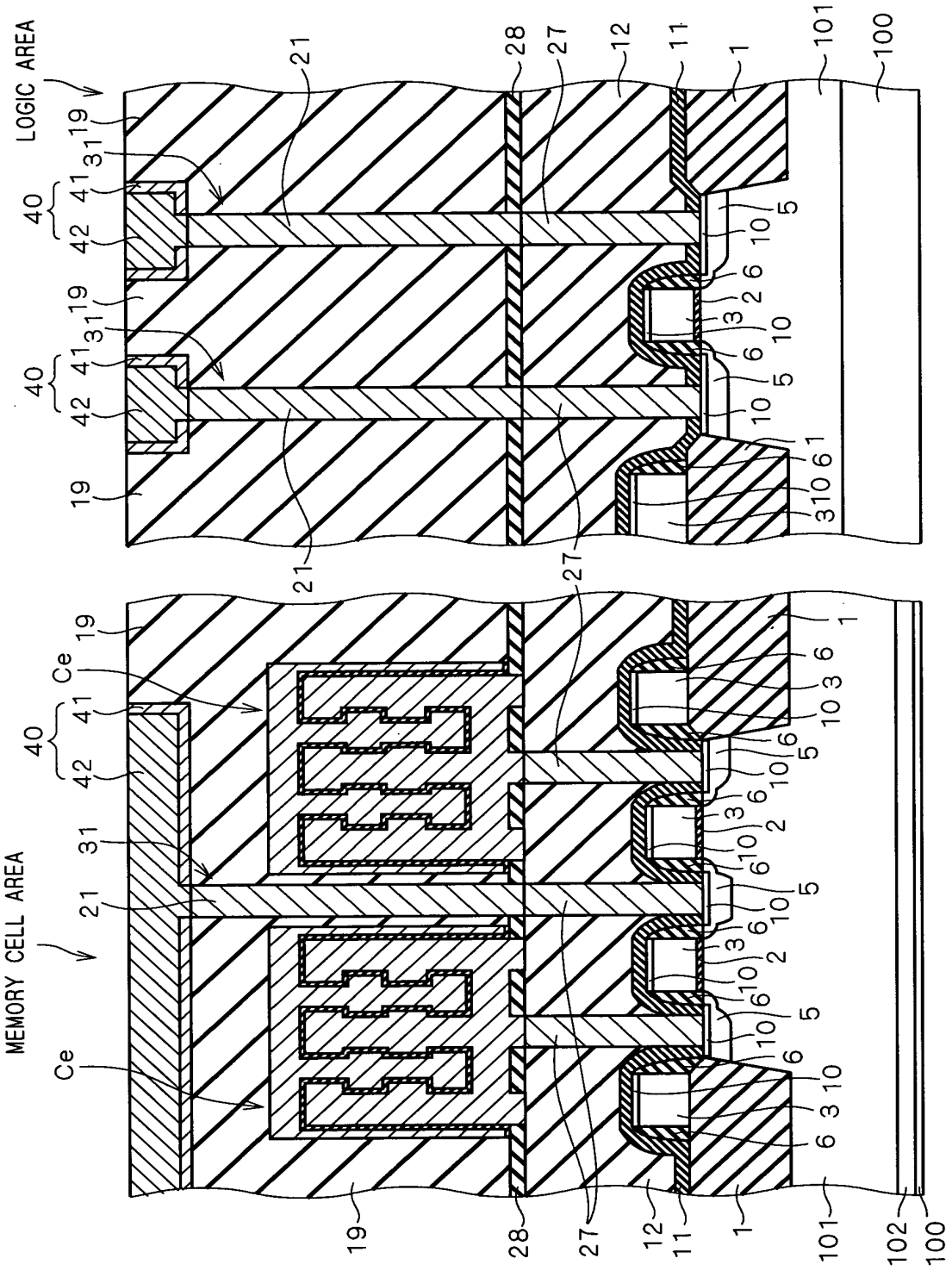

LOGIC AREA
MEMORY CELL AREA
Ce
19
21
28
27
12
11
1
101
100
102
40
41
42
31
5
10
6
3
2

FIG. 96

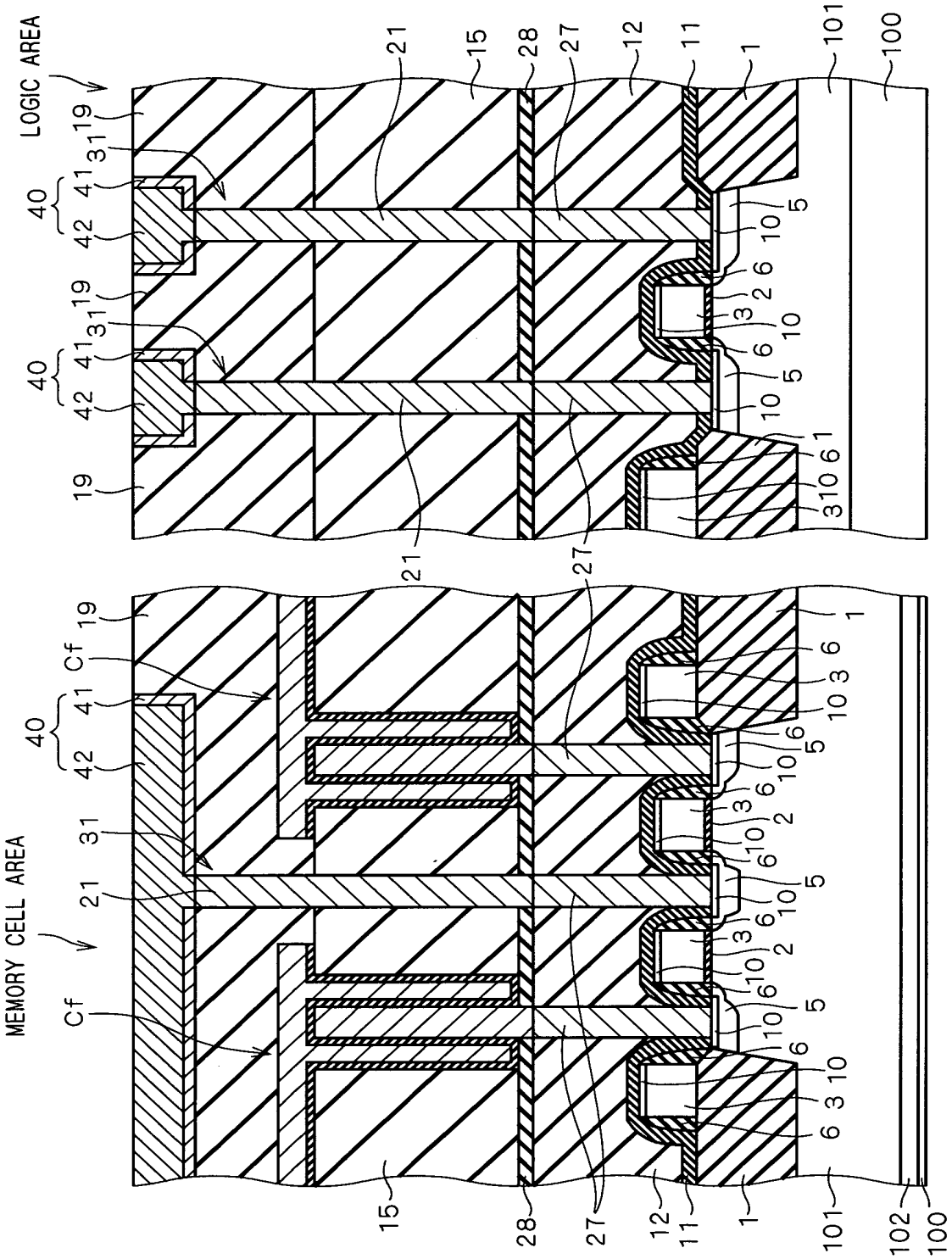

LOGIC AREA
MEMORY CELL AREA
Cf
19
31
40
41
42
21
15
28
27
12
11
1
101
100
102
5
10
6
2
3

FIG. 97

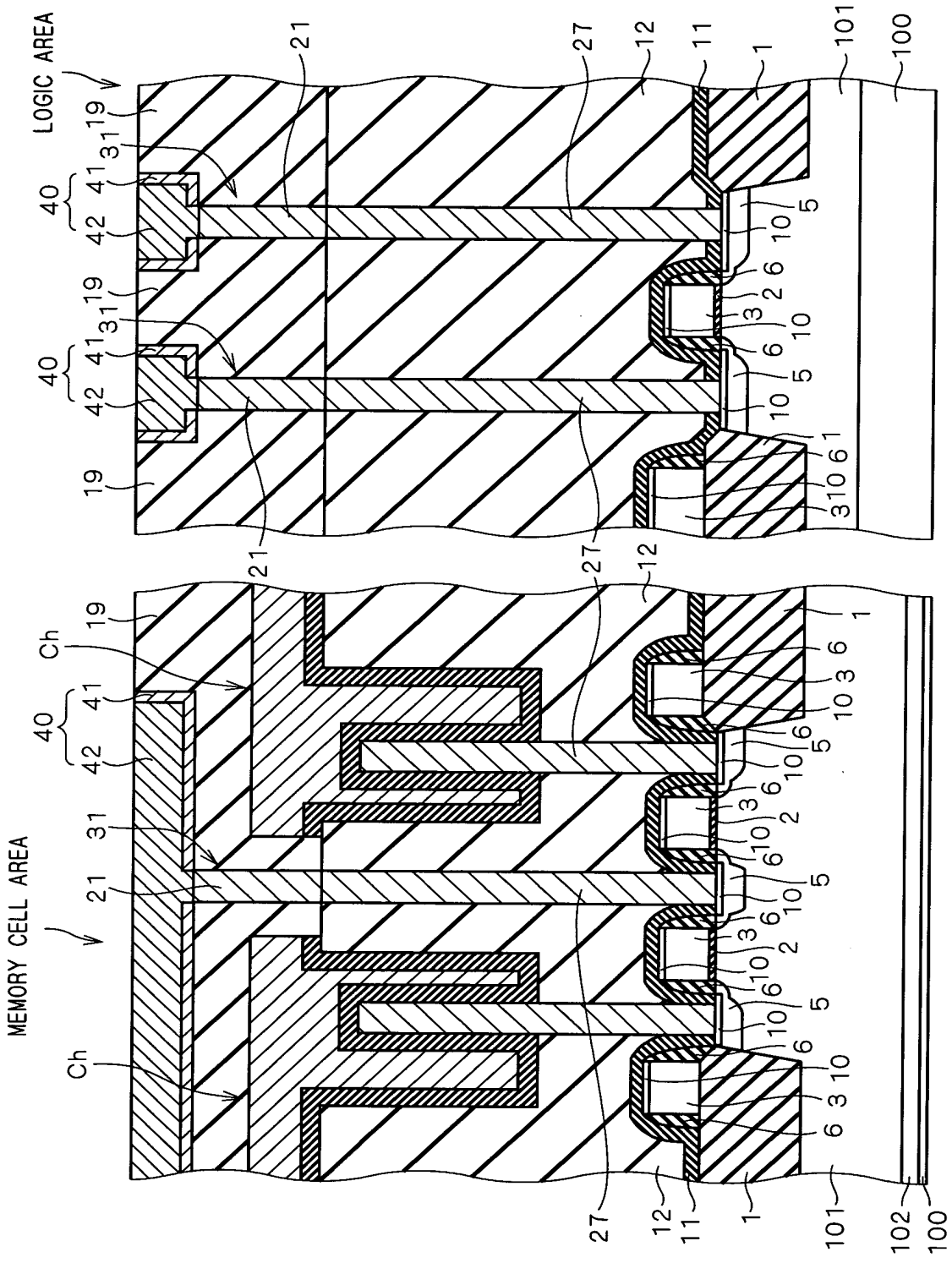
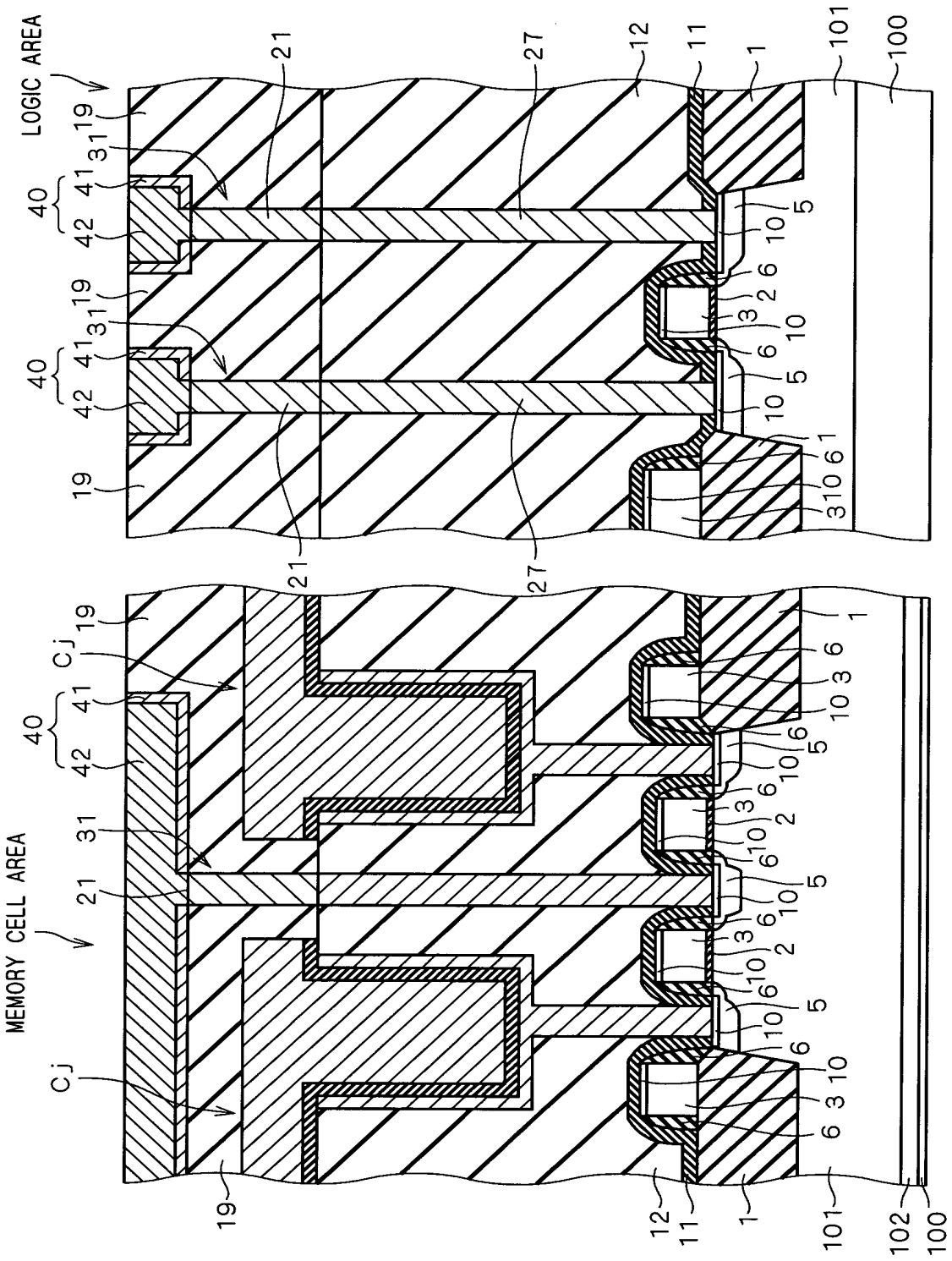

LOGIC AREA
MEMORY CELL AREA
Ch
19
31
40
41
42
21
27
12
11
1
101
102
100
5
10
6
3
2

FIG. 98


LOGIC AREA
MEMORY CELL AREA
19
31
40
41
42
21
27
12
11
1
101
100
102
Cj
10
6
5
3
2